



ZU-NEXUS-AI Kit - Evaluation board for the ATLAS ZUS3 SOM

Hardware user manual - KED-ZCU-DVK rev. V1 (PCB2026015)

Kairos Electronic Design - Hardware Develop Division

Sources: KED-ZCU-DVK-V1 schematic and ATLAS ZUS3 SOM documentation

Table of Contents

1. Overview

The ZU-NEXUS-AI Kit (KED-ZCU-DVK) is the reference carrier board for the ATLAS ZUS3 System-on-Module. It hosts the SOM in the SODIMM-260 socket J2 and demonstrates every module interface: M.2 PCIe Key-M, SYZYGY expansion, two PMOD ports, MIPI CSI-2 camera input, DisplayPort output, bootable microSD, Gigabit Ethernet, USB 3.0 Type-C dual-role and an integrated USB JTAG/UART debug chain. The board is also the reference implementation of the module power-sequencing rules (SOM_PWR_EN / SOM_PWR_OK handshake described in the ATLAS ZUS3 manual, section 3.5).



Figure 1 - The ZU-NEXUS-AI Kit with the ATLAS ZUS3 SOM installed in the SODIMM socket: RJ45, HDMI-size DisplayPort, USB and boot microSD on the left edge, PMOD headers on the front edge, M.2 slot area on the right.

Connector	Function	Detailed in
J3	5 V power jack (694103107102)	Section 2
J12	USB-C - JTAG / UART debug and alternative 5 V input	Sections 2, 12
J4	M.2 PCIe Key-M (2280/2240)	Section 4
J7	SYZYGY Standard pod/port (Samtec QSE-020)	Section 5
J10 / J11	PMOD expansion ports (2x6)	Section 6
J13	MIPI CSI-2 camera connector (22-pin FFC)	Section 7
J14	DisplayPort output, single lane	Section 8
J6	microSD card (boot)	Section 9
J5	Gigabit Ethernet RJ45	Section 10
J8	USB 3.0 Type-C dual-role port	Section 11
J9	TC2030 SWD header (SOM management MCU programming)	Section 12

2. Power input and sequencing (J3 / J12)

The board can be powered in two ways: through the barrel-jack J3 (694103107102, 5 V - 3 A, protected by the SMAJ5.0A TVS D3 and the B540C reverse diode D4, filtered by the common-mode choke L1) or through the USB-C debug connector J12 (VBUS). The two sources enter the TPS2121 power multiplexer U3, which selects the valid

one; the output (+5V_SWITCH) feeds the TPS25210 eFuse/hot-swap U1 that generates +5V_BOARD for the SODIMM (pins 251-259).

⚠ WARNING: Never exceed 5.5 V on the power input: 5.5 V is the absolute maximum supply voltage of the ATLAS ZUS3 module.

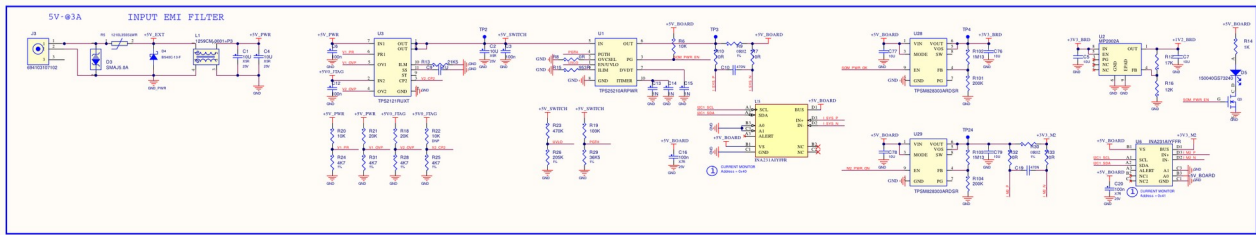


Figure 2 - Power input section: EMI filter and jack J3, TPS2121 source multiplexer (U3), TPS25210 eFuse (U1), 3.3 V bucks U28/U29, 1.2 V regulator U2 and the two INA231 current monitors (U5/U6).

The board implements the module power-up handshake exactly as prescribed: the eFuse power-good asserts SOM_PWR_EN automatically once the 5 V rail is stable, and the FPGA bank supplies are generated only when the module grants SOM_PWR_OK.

Function	Part	Notes
Source selection	U3 - TPS2121RUXT	Seamless mux between J3 jack and J12 USB-C VBUS, with OVP/priority resistor network
Inrush / protection	U1 - TPS25210ARPWR	eFuse on the 5 V rail; its Power Good drives SOM_PWR_EN (SODIMM 243) via Q3 - step 1 of the module sequencing
SOM_PWR_OK (SODIMM 247)	To U28 EN	The module consent enables buck U28 (+3V3_BRD = +VCCO_26) and, in cascade, regulator U2 (+1V2_BRD = +VCCO_65): the FPGA bank supplies rise only after SOM_PWR_OK, as required to avoid latch-up
+VCCO_26 (3.3 V)	U28 - TPSM828303	+3V3_BRD: SODIMM 63/64, PMOD VCC, SD card, camera supply and board logic
+VCCO_65 (1.2 V)	U2 - MP2002A	+1V2_BRD: SODIMM 101/102 and SYZYGY VIO (J7-39). 1.2 V suits both the MIPI D-PHY receiver of bank 65 and 1.2 V SYZYGY pods
M.2 slot supply	U29 - TPSM828303	+3V3_M2, enabled by the M2_PWR_ON PL signal (SODIMM 73, IO26_L9N)
Current monitors	U5 / U6 - INA231, 20 mOhm shunts	On I2C1: address 0x40 = system 5 V rail, address 0x41 = 3V3_M2 (M.2 slot)

Note: The +VCCO_26 and +VCCO_65 values are a choice of this carrier (3.3 V for HD bank 26, 1.2 V for HP banks 65/66). A custom baseboard may choose different bank voltages within the module specifications.

3. Boot mode, buttons and LEDs

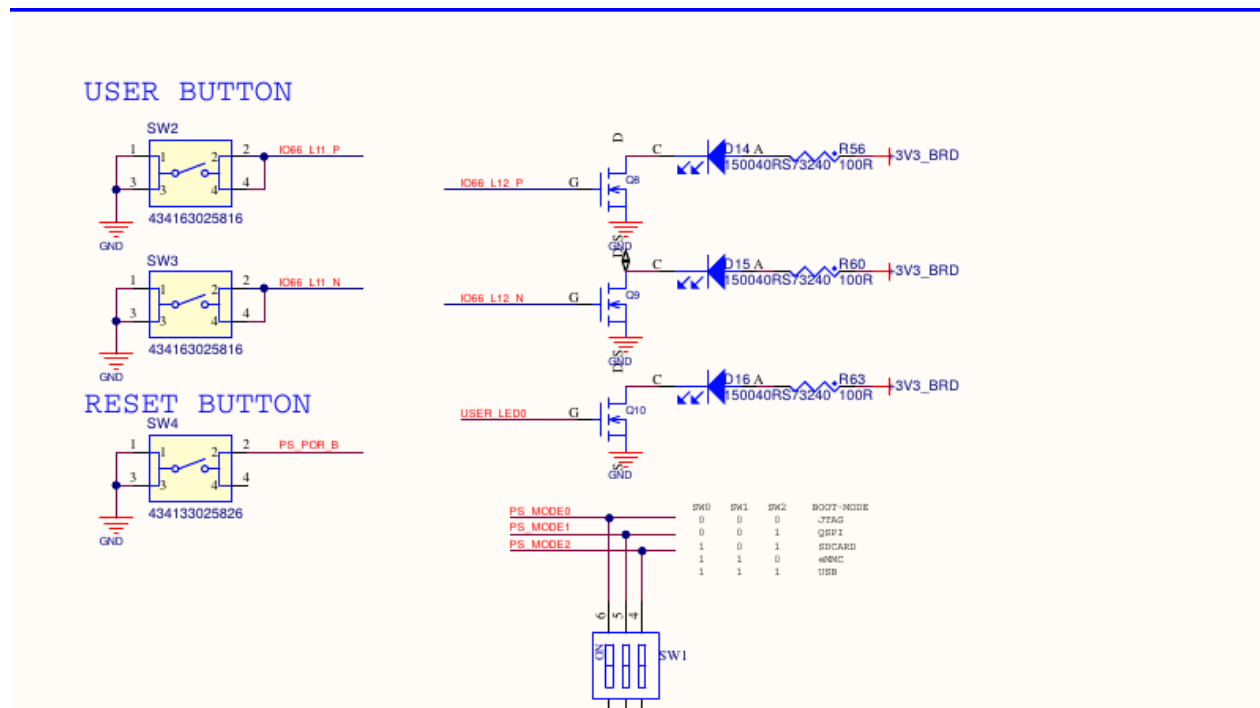


Figure 3 - User buttons SW2/SW3, reset button SW4, user LEDs D14/D15/D16 and boot-mode DIP switch SW1 with its coding table.

DIP switch SW1 straps the PS_MODE0..2 lines (SODIMM 236/238/240):

SW0	SW1	SW2	Boot mode
0	0	0	JTAG
0	0	1	QSPI
1	0	1	SD card
1	1	0	eMMC
1	1	1	USB

User I/O	Board part	SODIMM pin	SOM signal	FPGA ball (XDC)
User button SW2	SW2	109	IO66_L11P	B2
User button SW3	SW3	111	IO66_L11N	B1
User LED D14	Q8 + D14	110	IO66_L12P	A4
User LED D15	Q9 + D15	112	IO66_L12N	A3
User LED D16 (USER_LED0)	Q10 + D16	222	MIO37_PMU_GPO5	E11 (PS MIO)
Reset button SW4	SW4	249	SOM_SRSTn (DVK net PS_POR_B)	-

4. M.2 PCIe Key-M (J4)

Slot J4 (M.2 2280/2240, Key-M, with standoffs M1/M2) implements a PCIe x2 Gen1 Root Port using GT Lane0/Lane1 of the SOM. The PCIe reference clock is generated on the carrier by U9 (DSC557-0344, dual-output PCIe clock generator): output CLK0 feeds the M.2 slot REFCLK (through 33-ohm series resistors R49/R50) and output CLK1 feeds the SOM MGTR_REFCLK3 input (GTR_CLK3, Ref Clk3 in Vivado, 100 MHz), so slot and Root Port share the same reference. The DNP resistors R36/R42 allow the alternative use of the PCIe_REF_CLK output of the SOM. The reset PERST# and the CLKREQ# monitor pass through the SN74AVC2T245 level translator U8 (1.8 V module side, 3.3 V slot side).

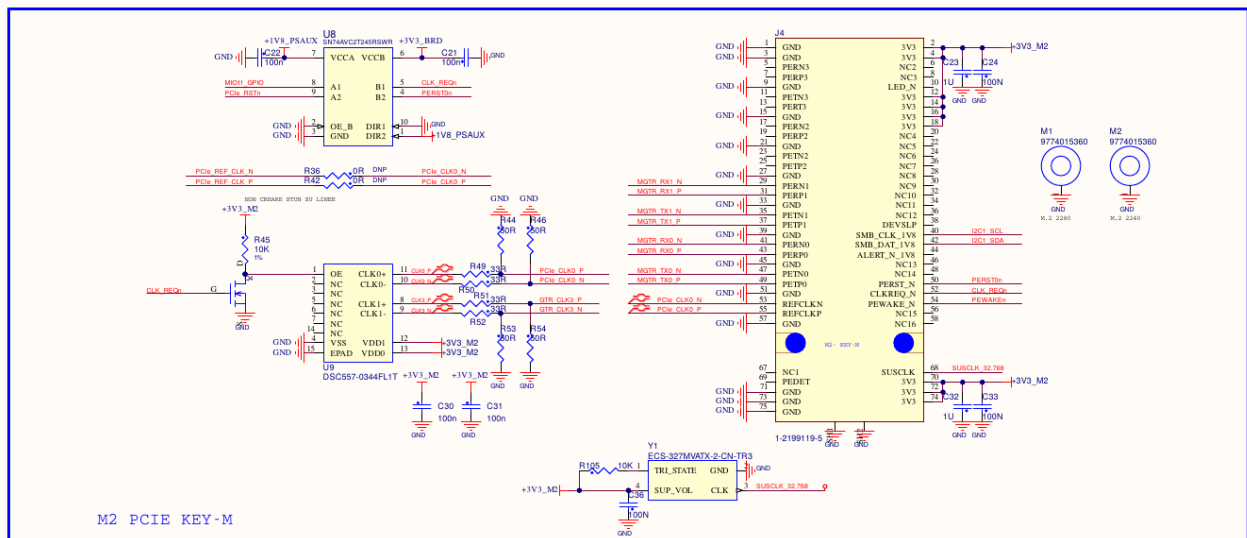


Figure 4 - M.2 Key-M section: slot J4, clock generator U9 (CLK0 to the slot, CLK1 to the SOM REFCLK3), level translator U8 for PERST#/CLKREQ#, 32.768 kHz SUSCLK oscillator Y1 and slot decoupling.

J4 pin	M.2 signal	Board net	SODIMM pin	SOM signal / MIO
41 / 43	PERn0 / PERp0	MGTR_RX0_N/P	52 / 54	GT Lane0 RX (PCIe lane 0)
47 / 49	PETn0 / PETp0	MGTR_TX0_N/P	58 / 60	GT Lane0 TX
29 / 31	PERn1 / PERp1	MGTR_RX1_N/P	40 / 42	GT Lane1 RX (PCIe lane 1)
35 / 37	PETn1 / PETp1	MGTR_TX1_N/P	46 / 48	GT Lane1 TX
53 / 55	REFCLKn / REFCLKp	PCle_CLK0_N/P	- (from U9 CLK0)	100 MHz slot reference; U9 CLK1 goes to SODIMM 35/37 (MGTR_REFCLK3)
50	PERST#	PERST0n (via U8)	59	MIO31_PClE_RSTn - PCIe reset from the PS
52	CLKREQ#	CLK_REQn (via U8/Q4)	61	MIO12 GPIO (DVK net MIO11_GPIO) - clock request monitor
54	PEWAKE#	R34 provision	-	Not connected by default
40 / 42	SMB_CLK / SMB_DAT	SMB_CLK_1V8 / SMB_DAT_1V8	223 / 225	MIO40 / MIO41 - I2C1, 1.8 V domain (shared with INA231 monitors and SYZGY)
68	SUSCLK	SUSCLK_32.768	- (Y1 on carrier)	32.768 kHz from oscillator Y1 (ECS-327MVATX)
3V3 pins	3V3	+3V3_M2 (U29)	73 (enable)	Slot power enabled by PL I/O IO26_L9N (M2_PWR_ON); current on INA231 0x41

5. SYZGY expansion (J7, Standard pod pinout)

J7 (Samtec QSE-020) follows the SYZGY Standard pod/port pinout: 8 differential pairs (or 16 single-ended I/Os) on PL bank 65, the SYZGY identification I2C bus, the RGA geographic-address resistor and VIO supplied by the carrier at the bank-65 voltage (+1V2_BRD, 1.2 V on this board). Use the FPGA ball column below as PACKAGE_PIN in the XDC/UCF, as in the module pinmux documentation.

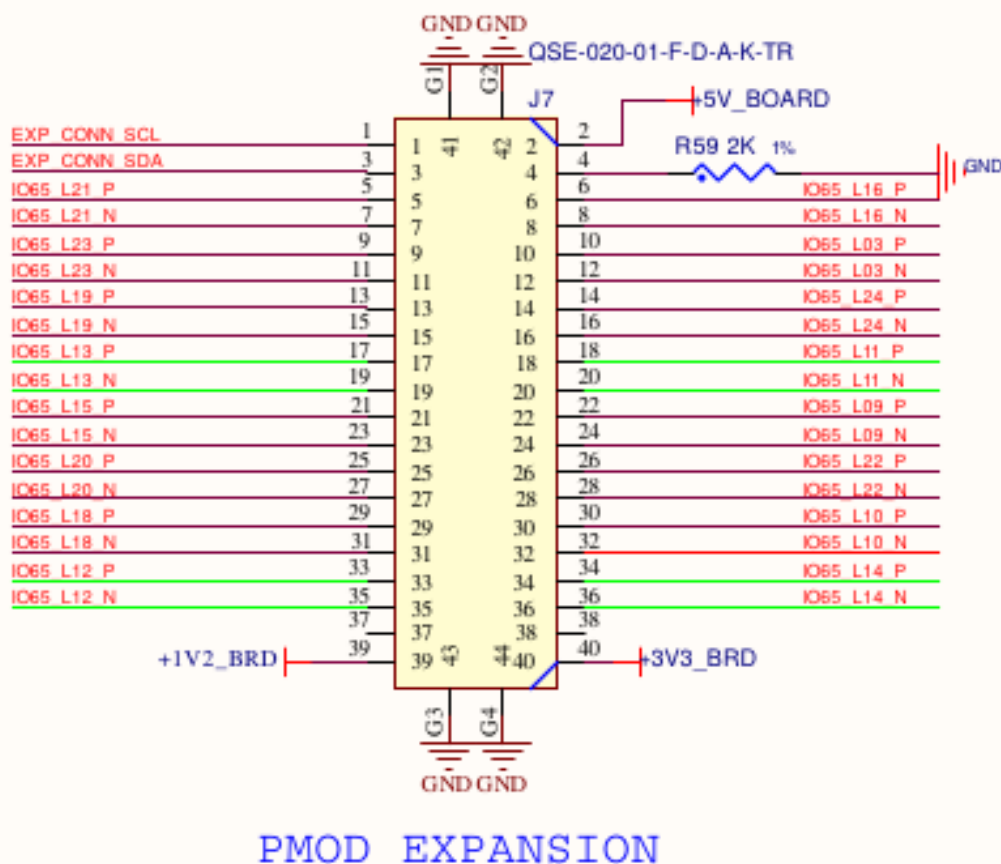


Figure 5 - SYZGY port J7: bank-65 differential pairs, identification I2C (EXP_CONN_SCL/SDA), RGA resistor R59 and supply pins (5V0, VIO = +1V2_BRD, 3V3).

J7 pin P / N	Board net	SODIMM P / N	SOM signal	FPGA ball P / N	AMD pin name (P side)	Clock
5 / 7	IO65_L21_P/N	121 / 123	IO65_L21P/N	E1 / D1	IO_L21P_T3L_N4_AD8P_65	-
9 / 11	IO65_L23_P/N	127 / 129	IO65_L23P/N	F3 / F2	IO_L23P_T3U_N8_I2C_SCLK_65	-
13 / 15	IO65_L19_P/N	133 / 135	IO65_L19P/N	G1 / F1	IO_L19P_T3L_N0_DBC_AD9P_65	DBC
17 / 19	IO65_L13_P/N	147 / 149	IO65_L13P/N	J3 / J2	IO_L13P_T2L_N0_GC_QBC_65	GC + QBC
21 / 23	IO65_L15_P/N	153 / 155	IO65_L15P/N	K1 / J1	IO_L15P_T2L_N4_AD11P_65	-
25 / 27	IO65_L20_P/N	134 / 136	IO65_L20P/N	E4 / E3	IO_L20P_T3L_N2_AD1P_65	-
29 / 31	IO65_L18_P/N	140 / 142	IO65_L18P/N	H4 / G4	IO_L18P_T2U_N10_AD2P_65	-
33 / 35	IO65_L12_P/N	160 / 162	IO65_L12P/N	L4 / L3	IO_L12P_T1U_N10_GC_65	GC
6 / 8	IO65_L16_P/N	148 / 150	IO65_L16P/N	J5 / H5	IO_L16P_T2U_N6_QBC_AD3P_65	QBC
10 / 12	IO65_L03_P/N	190 / 192	IO65_L03P/N	U2 / U1	IO_L3P_T0L_N4_AD15P_65	-
14 / 16	IO65_L24_P/N	122 / 124	IO65_L24P/N	D2 / C2	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	-

J7 pin P / N	Board net	SODIMM P / N	SOM signal	FPGA ball P / N	AMD pin name (P side)	Clock
18 / 20	IO65_L11_P/N	159 / 161	IO65_L11P/N	L2 / L1	IO_L11P_T1U_N 8_GC_65	GC
22 / 24	IO65_L09_P/N	165 / 167	IO65_L09P/N	M2 / M1	IO_L9P_T1L_N4_ AD12P_65	-
26 / 28	IO65_L22_P/N	128 / 130	IO65_L22P/N	D3 / C3	IO_L22P_T3U_N 6_DBC_AD0P_65	DBC
30 / 32	IO65_L10_P/N	166 / 168	IO65_L10P/N	M5 / M4	IO_L10P_T1U_N 6_QBC_AD4P_6 5	QBC
34 / 36	IO65_L14_P/N	154 / 156	IO65_L14P/N	K4 / K3	IO_L14P_T2L_N2 _GC_65	GC

J7 service pin	Function	Connection
1 / 3	SYZGY I2C SCL / SDA	EXP_CONN_SCL / EXP_CONN_SDA - PL I/Os IO26_L11N (SODIMM 67, ball B5) and IO26_L9P (SODIMM 71, ball B9)
2	5V0	+5V_BOARD
4	RGA (geographic address)	2 kOhm resistor R59 to GND
39	VIO	+1V2_BRD = +VCCO_65 (bank-65 voltage, 1.2 V)
40	3V3	+3V3_BRD

6. PMOD ports (J10 / J11)

Two standard 2x6 PMOD ports on PL bank 26 (HD bank, 3.3 V on this board since +VCCO_26 = +3V3_BRD). FPGA ball = value for PACKAGE_PIN in the XDC/UCF.

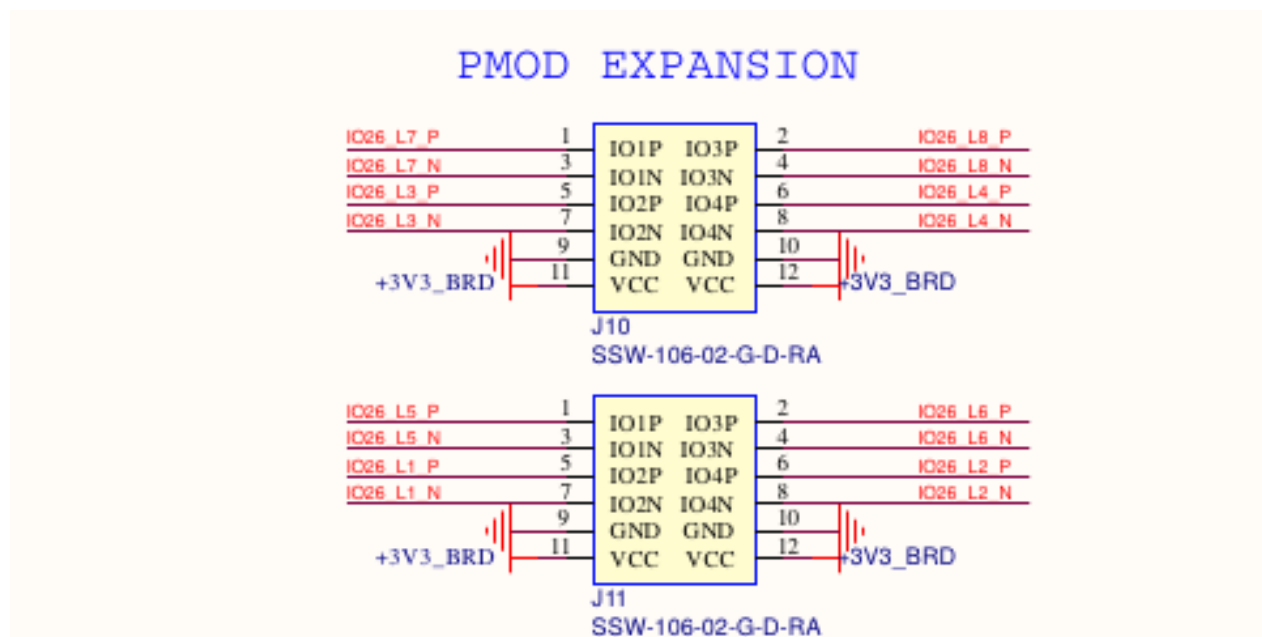


Figure 6 - PMOD ports J10/J11 on bank-26 I/Os, with GND and +3V3_BRD supply pins.

PMOD A - J10:

J10 pin	SODIMM pin	SOM signal	FPGA ball (XDC)	AMD pin name	Clock
1	77	IO26_L7P	D5	IO_L7P_HDGC_AD5 P_26	HDGC
2	78	IO26_L8P	C8	IO_L8P_HDGC_AD4 P_26	HDGC
3	79	IO26_L7N	C5	IO_L7N_HDGC_AD5 N_26	HDGC
4	80	IO26_L8N	C7	IO_L8N_HDGC_AD4 N_26	HDGC
5	89	IO26_L3P	E6	IO_L3P_AD9P_26	-

J10 pin	SODIMM pin	SOM signal	FPGA ball (XDC)	AMD pin name	Clock
6	90	IO26_L4P	F8	IO_L4P_AD8P_26	-
7	91	IO26_L3N	E5	IO_L3N_AD9N_26	-
8	92	IO26_L4N	F7	IO_L4N_AD8N_26	-
9 / 10	-	GND	-	-	-
11 / 12	-	+3V3_BRD (VCC)	-	-	-

PMOD B - J11:

J11 pin	SODIMM pin	SOM signal	FPGA ball (XDC)	AMD pin name	Clock
1	83	IO26_L5P	D7	IO_L5P_HDGC_AD7P_26	HDGC
2	84	IO26_L6P	E8	IO_L6P_HDGC_AD6P_26	HDGC
3	85	IO26_L5N	D6	IO_L5N_HDGC_AD7N_26	HDGC
4	86	IO26_L6N	D8	IO_L6N_HDGC_AD6N_26	HDGC
5	95	IO26_L1P	G6	IO_L1P_AD11P_26	-
6	96	IO26_L2P	G7	IO_L2P_AD10P_26	-
7	97	IO26_L1N	G5	IO_L1N_AD11N_26	-
8	98	IO26_L2N	F6	IO_L2N_AD10N_26	-
9 / 10	-	GND	-	-	-
11 / 12	-	+3V3_BRD (VCC)	-	-	-

7. MIPI camera connector (J13)

J13 (22-pin FFC, Raspberry-Pi camera compatible) brings a 4-lane MIPI CSI-2 D-PHY receiver into PL bank 65, which on this board runs at 1.2 V (+VCCO_65 = +1V2_BRD) as required by the D-PHY receiver. The clock lane lands on a QBC (byte-clock capable) pair, as required by the AMD MIPI D-PHY RX implementation; the module reference Vivado design (MIPI CSI-2 RX subsystem) uses exactly these pins. Control signals (camera power-down and camera I2C) are on bank 26.

MIPI CAMERA CONNECTOR

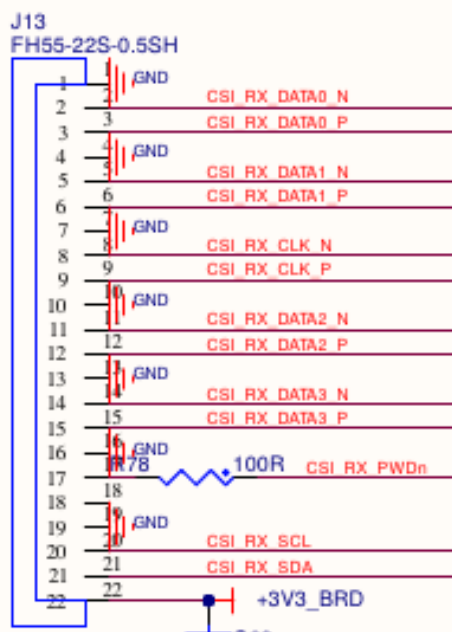


Figure 7 - MIPI camera connector J13: four CSI-2 data lanes plus clock on bank-65 pairs, camera control (PwDn, SCL, SDA) on bank 26, 3.3 V camera supply.

J13 pin	CSI-2 signal	SODIMM pin	SOM signal	FPGA ball (XDC)	AMD pin name
3 / 2	DATA0 P / N	183 / 185	IO65_L02P/N	P3 / R3	IO_L2P_T0L_N2_65 / IO_L2N_T0L_N3_65
6 / 5	DATA1 P / N	177 / 179	IO65_L06P/N	P5 / R5	IO_L6P_T0U_N10_A D6P_65 / IO_L6N_T0U_N11_ AD6N_65
9 / 8	CLK P / N	171 / 173	IO65_L07P/N	N2 / P1	IO_L7P_T1L_N0_QB C_AD13P_65 / IO_L7N_T1L_N1_QB C_AD13N_65 (QBC)
12 / 11	DATA2 P / N	184 / 186	IO65_L01P/N	T3 / T2	IO_L1P_T0L_N0_DB C_65 / IO_L1N_T0L_N1_DB C_65
15 / 14	DATA3 P / N	178 / 180	IO65_L05P/N	R1 / T1	IO_L5P_T0U_N8_AD 14P_65 / IO_L5N_T0U_N9_A D14N_65
17	CAM_PwDn (via R78)	66	IO26_L12P	B7	IO_L12P_AD0P_26
20	CAM_SCL	68	IO26_L12N	A6	IO_L12N_AD0N_26
21	CAM_SDA	72	IO26_L10P	A8	IO_L10P_AD2P_26
22	3.3 V camera supply	-	+3V3_BRD	-	-
1,4,7,10,13,16,19	GND	-	GND	-	-

8. DisplayPort output (J14)

J14 (full-size DisplayPort, single lane) is driven by the SOM DisplayPort controller: main link on GT Lane3, AUX channel and HPD through the PS MIO pins, level-translated on the carrier (U20/U30) and AC-coupled/protected through U16. DP_PWR (pin 20) is switched by the TPS2552 U18. MIO pins used:

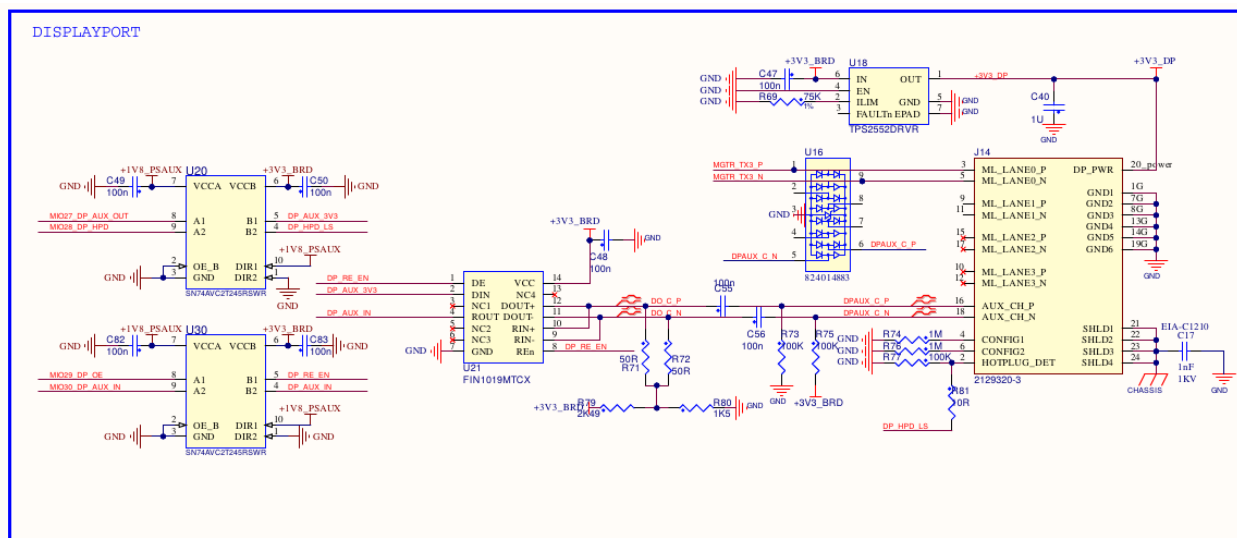


Figure 8 - DisplayPort section: main-link AC coupling and ESD (U16), AUX-channel bias network and level translators (U20/U30), HPD conditioning and DP_PWR switch U18.

Function	SODIMM pin	MIO	J14 pin
Main link lane 0 (MGTR_TX3_P/N)	6 / 4	- (GT Lane3)	3 / 5 (ML_LANE0_P/N)
DP AUX out	32	MIO27_DP_AUX_OUT	16 / 18 (AUX_CH via U20 + coupling)
DP AUX in	30	MIO30_DP_AUX_IN	16 / 18
DP AUX output enable	28	MIO29_DP_OE	- (direction control of U20/U30)
Hot-plug detect	34	MIO28_DP_HPD	2 (HPD, level-shifted)
DP_PWR 3.3 V	-	-	20 (via U18 TPS2552, +3V3_DP)

9. microSD card (J6)

J6 is the boot/storage microSD slot, connected to the SD1 controller of the SOM. Since the module MIO bank runs at 1.8 V, the board inserts the TXS02612 SDIO level translator U10 (1.8 V to 3.3 V); Card Detect is buffered by Q7 and every card line is ESD-protected. Write Protect (MIO44) is only brought to test point TP6 (the microSD form factor has no WP contact). MIO pins used:

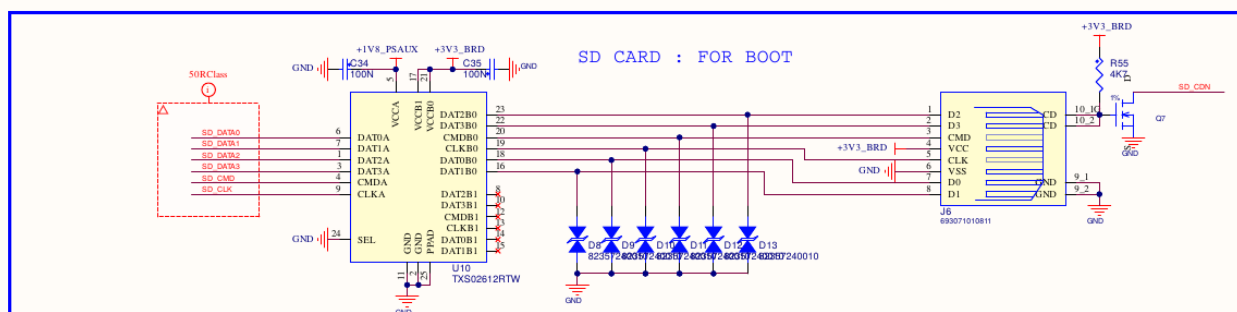


Figure 9 - microSD section: TXS02612 level translator U10 between the 1.8 V module signals and the 3.3 V card, ESD diodes and Card Detect buffer Q7.

Function	SODIMM pin	MIO	Path on the board
SD DATA0..3	211 / 213 / 203 / 205	MIO46 / 47 / 48 / 49	U10 TXS02612 -> J6 with ESD diodes
SD CMD	207	MIO50	U10 -> J6

Function	SODIMM pin	MIO	Path on the board
SD CLK	209	MIO51	U10 -> J6
Card Detect	217	MIO45_SD_CDN	J6 CD switch via Q7
Write Protect	215	MIO44_SD_WPn	Test point TP6 only

Note: To boot from SD card set SW1 = 101 (section 3).

10. Gigabit Ethernet (J5)

J5 (RJ45) carries the MDI side of the on-module KSZ9031RNX PHY through the discrete magnetics T1; the carrier adds only magnetics, termination/EMC network and the two status LEDs (driven by Q5/Q6). The RGMII interface stays inside the module. Signals used:

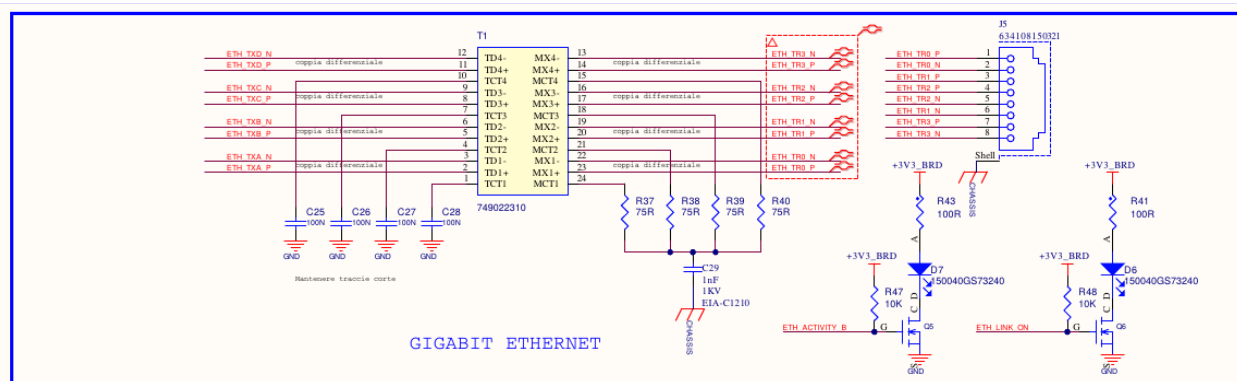


Figure 10 - Gigabit Ethernet section: discrete magnetics T1 between the module MDI pairs and the RJ45 J5, Bob-Smith termination network and link/activity LED drivers.

Function	SODIMM pin	MIO / signal	J5 / T1
MDI pair A	5 / 7	- (PHY MDI)	T1 -> J5 1/2
MDI pair B	11 / 13	- (PHY MDI)	T1 -> J5 3/6
MDI pair C	17 / 19	- (PHY MDI)	T1 -> J5 4/5
MDI pair D	23 / 25	- (PHY MDI)	T1 -> J5 7/8
Link LED	29	ETH_LINK_ON	LED via Q6
Activity LED	31	ETH_ACTIVITY_B	LED via Q5
Magnetics center-tap	1	+3V3_ETH	T1 center taps
RGMII + MDIO (inside SOM)	-	MIO64..75 (GEM3), MIO76/77 (MDC/MDIO)	-

11. USB 3.0 Type-C dual-role port (J8)

J8 is a USB Type-C dual-role port combining the SOM USB 2.0 line side (OTG_D_P/N, SODIMM 49/47, through common-mode choke L2) and the USB 3.0 SuperSpeed lane (GT Lane2: SODIMM 16/18 TX, 22/24 RX). The HD3SS3212 mux U13 handles the Type-C plug orientation on the SuperSpeed pairs, the TUSB322 CC controller U12 negotiates the role and drives OTG_ID (SODIMM 57); VBUS sense goes to SODIMM 51 and VBUS sourcing is switched by the TPS2552 U11 (enabled by OTG_CPEN, SODIMM 53).

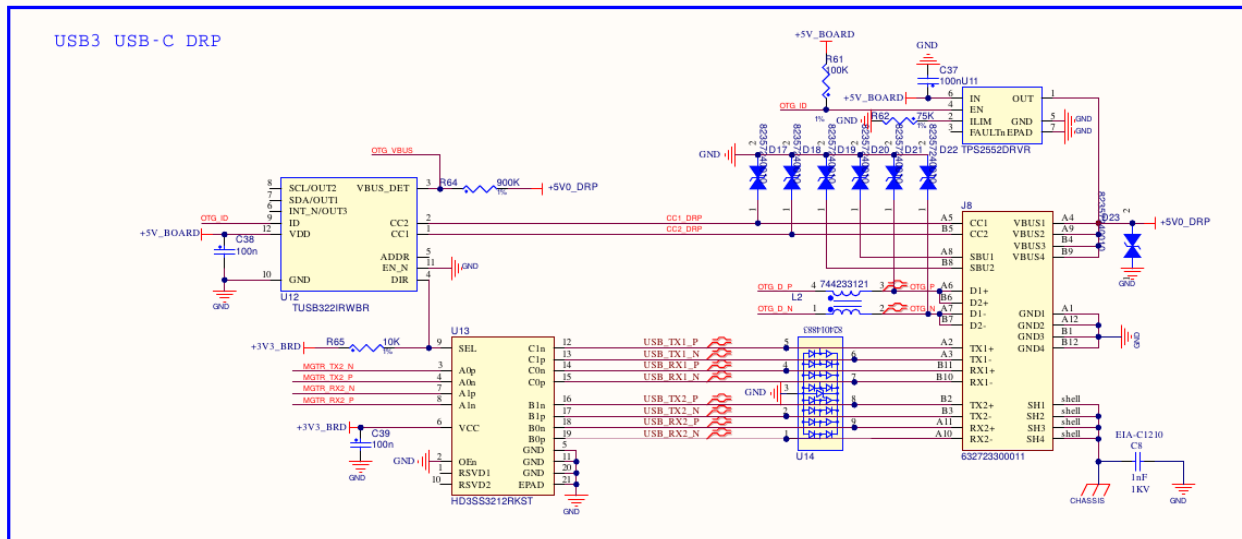


Figure 11 - USB 3.0 Type-C section: TUSB322 CC controller (U12), HD3SS3212 SuperSpeed mux (U13), VBUS switch (U11), common-mode chokes and ESD protections.

12. USB JTAG / UART debug (J12) and MCU SWD header (J9)

J12 (USB-C) connects the FT4232H quad USB bridge U17 (with its M93C66 configuration EEPROM U24): channel A implements the JTAG chain through SN74AVC2T245 translators towards SODIMM 224/226/228/230 (JTAG_TCK/TMS/TDI/TDO), plus the PS_SRST_B line (232) and the module system reset SOM_SRSTn (249, DVK net PS_POR_B, shared with push-button SW4); channel B is the PS UART0 console (MIO10/11, SODIMM 212/214); channel C is the service UART of the module management MCU (SODIMM 256/258). The same connector can power the board (section 2). J9 (Tag-Connect TC2030) is the production SWD header for the module management MCU: SWDIO (252), SWCLK (254), MCU_RSTn (250).

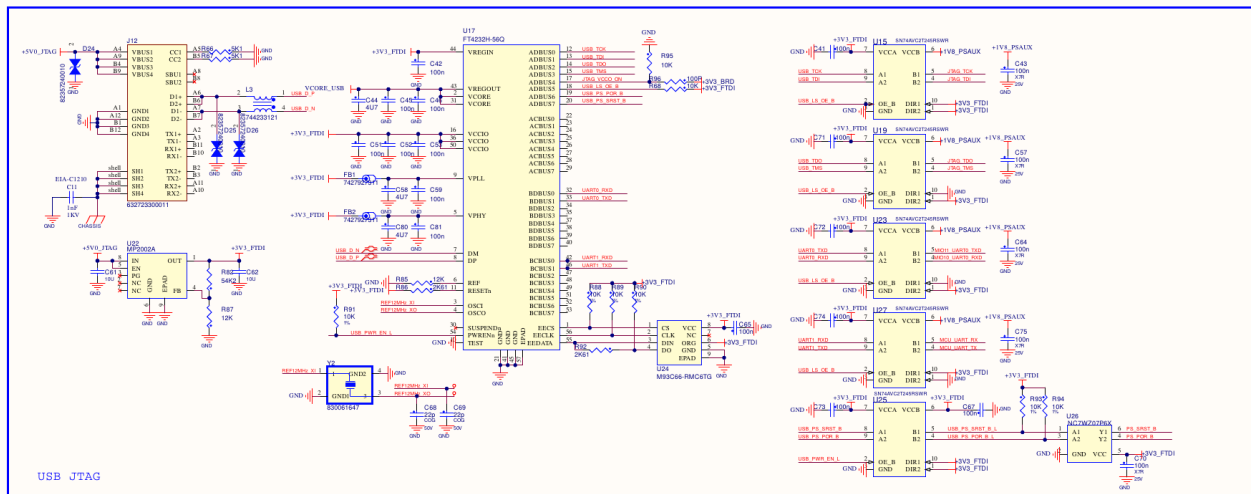


Figure 12 - USB JTAG/UART section: FT4232H bridge U17 with EEPROM, level translators towards the JTAG chain, the two UARTs and the reset lines; TC2030 SWD header J9 for MCU production programming.