ATLAS ZUS3 SOM - Zynq UltraScale+ ZU1EG (SODIMM-260)

Architecture, power, SODIMM connector pinout and Vivado configuration manual

Kairos Electronic Design - Hardware Develop Division

Sources: ked_zcu_sodimm4 schematic (rev. A) and ZCU-DM-X1-R0 Vivado project (Vivado 2022.2)

Table of Contents

1. Introduction

The ATLAS ZUS3 SOM (project code ZCU-DM-X1) is a 260-pin SODIMM System-on-Module based on the AMD Zynq UltraScale+ MPSoC XCZU1EG (SBVA484 package, speed grade -1, Vivado part xczu1eg-sbva484-1-e). The module integrates on its PCB every resource needed for stand-alone operation of the device: switching and linear power supplies, 32-bit LPDDR4 memory, eMMC memory, QSPI flash, Gigabit Ethernet PHY, USB 2.0 ULPI PHY, a programmable clock generator for the GTR transceiver references and a power-management microcontroller (MCU).

Figure 1 - The ATLAS ZUS3 SOM module (top side): Zynq UltraScale+ (U14), LPDDR4 (U16), eMMC (U21), management MCU (U25) and SODIMM edge connector.

The SODIMM edge connector (260-pin, PCB2 in the schematic) exposes to the customer baseboard: the input and service power rails, the Programmable Logic I/Os (banks 26, 65 and 66), the Processing System MIO signals routed to the peripherals (SD card, CAN, UART, I2C, DisplayPort AUX, PMU GPO), the four GTR lanes (PCIe x2, USB 3.0, DisplayPort), the Ethernet MDI interface, the USB 2.0 line side, the JTAG chain, the boot-mode signals and the power control/monitor signals. The SOM is a generic module: the customer develops a custom baseboard, freely assigning the PL I/Os available on the edge connector.

⚠ WARNING: THERMAL DISSIPATION: the module must be operated with adequate cooling (heatsink and/or airflow, designed by the carrier/system integrator) so that the junction temperature of the Zynq UltraScale+ never exceeds the maximum rating specified by AMD for the device grade (100 deg C for commercial grade - see AMD DS891/DS926). Monitor the die temperature at runtime through SYSMON.

This document describes the module architecture, the power section, the clock distribution, the MIO pin assignment of the PS peripherals with the corresponding settings of the reference Vivado project (ZCU-DM-X1-R0.tcl, Vivado 2022.2), and provides the complete 260-pin connector table with, for PL pins, the FPGA ball, the pin name according to the AMD pinout and the clock capability (Global Clock / Byte Clock); for PS pins it lists the FPGA pin, the bank it belongs to and the FPGA pin name.

2. Module architecture

The heart of the module is the Zynq UltraScale+ ZU1EG (U14): quad-core ARM Cortex-A53 (1200 MHz in the reference project), dual-core Cortex-R5 (500 MHz), PMU, and Programmable Logic. Around the device the module integrates the following main blocks:

Block	Reference	Description
MPSoC	U14 (XCZU1EG-SBVA484)	Processing System + Programmable Logic; PL banks 26/65/66 exposed on the connector
LPDDR4	U16 (NT6AN512T32AV-J2)	16 Gbit (512M x 32) LPDDR4, 32-bit bus on PS DDR bank 504, 240 ohm ZQ termination

Block	Reference	Description
eMMC	U21 (EMMC08G-W325-X03U)	8 GByte e.MMC on the SD0 controller, 8-bit bus (MIO13-22)
QSPI flash	U22 (MT25QU512ABB8E12)	512 Mbit 1.8 V QSPI on MIO0-5 (controller disabled in the reference project)
Ethernet PHY	U18 (KSZ9031RNX)	Gigabit Ethernet RGMII on GEM3 (MIO64-75) + MDIO (MIO76-77); MDI side on the connector
USB 2.0 PHY	U20 (USB3320C-EZK)	ULPI PHY for USB0 (MIO52-63); D+/D-, VBUS, ID, CPEN on the connector
Clock generator	U15 (5P49V6965)	I2C0-programmable VersaClock; generates the GTR references (USB3 26 MHz, DP 27 MHz, SATA 125 MHz, PCIe 100 MHz)
Management MCU	U25 (ATSAML11E16A)	Power sequencing and monitoring, power-up handshake with the baseboard, service UART and SWD on the connector
Reset supervisor	U24 (TPS3808G33) + U23 (SN74AHC1G08)	PS_POR_B generation and system reset combination
Regulators	U1, U5, U10, U12, U9, U13, U4	See chapter 3 - Power section
MAC EEPROM	U19 (24AA02E48-TSOT)	Unique MAC address on the I2C0 bus
Oscillators	Y1, Y2, Y3, Y4, Y5	33.3333 MHz PS_REF_CLK, 32.768 kHz RTC, 25 MHz clock-gen, 24 MHz USB PHY, 25 MHz Ethernet PHY

All PS MIO banks (500, 501, 502) are powered at 1.8 V (LVCMOS18, as set in the TCL: PSU_BANK_0/1/2_IO_STANDARD = LVCMOS18); the MIO signals exposed on the connector are therefore 1.8 V level. An important architectural choice: the supply of the PL I/O banks is NOT defined on the SOM. The bank supply pins +VCCO_26 and +VCCO_65 are brought out on the SODIMM connector, so the bank voltages (and therefore the I/O standards) are defined entirely from the outside, by the baseboard. Bank 66 shares the bank-65 supply through the +VCCO_65 rail. See section 3.5 for the mandatory sequencing rules that apply to these rails.

3. Power section

The module is powered from a single +5V_BOARD rail supplied by the baseboard on SODIMM pins 251-259. From this rail the on-board regulators generate all the MPSoC and peripheral voltages. Power sequencing and monitoring are handled by microcontroller U25.

⚠ **WARNING: ABSOLUTE MAXIMUM SUPPLY: the maximum module supply voltage is 5.5 V and must NEVER be exceeded on +5V_BOARD, under any transient or steady-state condition.**

Figure 2 - ATLAS ZUS3 power distribution tree: each regulator and the sections it powers. The +VCCO_26/+VCCO_65 rails (red, right) come from the carrier and must be gated by SOM_PWR_OK.

3.1 Main switching regulators

Reg.	Part	Input	Output	Generated rails / loads
U1	TPS62872 (buck, sync out, I2C)	+5V_BOARD	0.85 V	+0V85_PSINTLP, +0V85_PS_INTFP, +0V85_PL_INT, +0V85_PL_BRAM (PS and PL core); +0V85_MGTRAVCC through ferrite FB6. Power good: PG_0V85
U5	MPM3834C (buck module)	+5V_BOARD	1.8 V	+1V8_PSAUX, +1V8_PS, +1V8_PL; +1V8_MGTRAVTT (FB5) and +1V8_PSDDR_PLL (FB4). Power good: PG_1V8
U10	MPM3834C (buck module)	+5V_BOARD	1.1 V	+1V1_PS_DDR: LPDDR4 supply (VDD2/VDDQ) and PS DDR bank 504 (VCCO_PSDDR). Power good: PG_1V1
U12	MPM3834C (buck module)	+5V_BOARD	3.3 V	+3V3_PS: module 3.3 V rail (supervisor, LEDs, pull-ups, +3V3_ETH via ferrite). Power good on the SOM_PWR_OK network

U1 is the core regulator: it delivers the 0.85 V to the PS (VCC_PSINTLP, VCC_PSINTFP) and PL (VCCINT, VCCINT_IO, VCCBRAM) through partitioning ferrites (FB4, FB5, FB6 on sheet 4) that split the PS, PL and MGTRAVCC domains for filtering. The TPS62872 is I2C-configurable (MIO38/39 I2C0 lines with pull-ups) and has MODE/VSEL/FSEL pins strapped with resistors on the module; the power inductor is L3 (110 nH).

U5 generates the 1.8 V domain, split into +1V8_PSAUX (VCC_PSAUX, MIO banks, auxiliary circuitry), +1V8_PS and +1V8_PL (VCCAUX), plus the filtered rails +1V8_MGTRAVTT (transceiver terminations) and +1V8_PSDDR_PLL

(DDR controller PLL). U10 provides the 1.1 V LPDDR4 rail (memory and MPSoC bank 504). U12 generates the module 3.3 V.

3.2 Linear regulators

Reg.	Part	Input	Output	Function
U9	LDLN025PU12R (low-noise LDO)	+1V8_PSAUX	+1V2_PSPLL	Low-noise supply of the PS PLLs (VCC_PSPLL)
U13	NCV8114ASN120T1G	+3V3_PS	+1V2_ETH	1.2 V core of the KSZ9031RNX Ethernet PHY
U4	NCV8114ASN180T1G	+5V_BOARD	+1V8_MCU	Supply of microcontroller U25; level reference of the MCU signals on the connector (pin 260)

3.3 Power-management MCU (U25 - ATSAML11E16A)

Microcontroller U25 is the sequencer and supervisor of the module power supplies. Its main functions are:

Function	Signals involved	Description
Power enable	EN_PWR, SOM_PWR_EN (pin 243)	On reception of SOM_PWR_EN from the baseboard the MCU enables the regulators in sequence through the EN_PWR line
Power-good check	PG_0V85, PG_1V8, PG_1V1	The MCU waits for the regulator power-good signals before declaring the module valid
Rail voltage readout	ADC1-ADC4 (4k7/4k7 dividers)	Four ADC inputs read the +0V85_PSINTLP, +1V8_PSAUX, +1V1_PS_DDR and +3V3_PS rails through resistive dividers; the readings are available on the service UART
Baseboard handshake	SOM_PWR_ON (245), SOM_PWR_OK (247), SOM_SRSTn (249)	SOM_PWR_OK tells the baseboard that all voltages are valid; SOM_SRSTn allows the system reset; BAT46AW diodes protect the handshake lines
MPSoC PMU interface	MIO32_PMU_GPO0, MIO33_PMU_GPO1, MIO26_PMU_INPUT, MIO38/39 I2C0	The MCU talks to the MPSoC PMU for boot status and shutdown requests
Carrier-side service	MCU_UART1_TX/RX (256/258), SWDIO/SWCLK (252/254), MCU_RSTn (250)	Service UART (power log, commands) and SWD port to update the MCU firmware from the baseboard

Supervisor U24 (TPS3808G33) monitors the 3.3 V/1.8 V rail and generates PS_POR_B towards the MPSoC; AND gate U23 combines PS_SRST_B coming from the connector (pin 232) with the internal reset network (RESET_B) so that both the baseboard and the MCU can reset the system. Status LEDs D4 (green, PS_ERR_ST), D5 (red, PS_ERR_OUT) and D6 (blue, PS_DONE) report the MPSoC configuration and error status.

3.4 Rails on the SODIMM connector

Pin	Rail	Direction	Notes
251, 253, 255, 257, 259	+5V_BOARD	Input	Main module supply
63, 64	+VCCO_26	Input	PL bank 26 (HD) VCCO: 1.2 V - 3.3 V, customer's choice
101, 102	+VCCO_65	Input	PL banks 65/66 (HP) VCCO: 1.0 V - 1.8 V, customer's choice
242	+1V5_PSBATT	Input	PS RTC battery (VCC_PSBATT), through ferrite FB7
36, 201, 202	+1V8_PSAUX	Output	1.8 V auxiliary for pull-ups and service logic on the carrier - maximum external load 350 mA
1	+3V3_ETH	Output	3.3 V for the Ethernet magnetics center-tap on the carrier
260	+1V8_MCU	Output	Level reference of the MCU

Pin	Rail	Direction	Notes
			signals - maximum external load 100 mA
239, 241	ADC_V_P / ADC_V_N	Input	SYSMON differential analog channel (VP/VN, 0-1 V)

3.5 Power sequencing: SOM_PWR_EN / SOM_PWR_OK / SOM_PWR_ON

⚠ **WARNING: CRITICAL - RISK OF FPGA LATCH-UP: the FPGA I/O banks must NOT receive any supply until the PL core is powered. The baseboard must keep +VCCO_26 and +VCCO_65 OFF (and every signal driven into the SOM inactive/3-stated) until the SOM asserts SOM_PWR_OK. Applying VCCO or driving I/Os before SOM_PWR_OK grants consent can trigger latch-up of the FPGA and permanently damage the module.**

The power-up of the module is a two-way handshake between the baseboard and the SOM, built on three SODIMM signals:

Signal	SODIMM pin	Direction	Electrical type	Meaning
SOM_PWR_EN	243	Baseboard to SOM	1.8 V logic input	The baseboard asserts it to tell the SOM that the 5 V supply is stable and the module may start its power-up sequence
SOM_PWR_OK	247	SOM to baseboard	Open-collector, active high (external pull-up required on the carrier)	Asserted by the SOM when the internal sequencing is complete: it is the consent to enable the FPGA bank supplies (+VCCO_26, +VCCO_65) on the baseboard
SOM_PWR_ON	245	Baseboard to SOM (MCU)	1.8 V logic, to MCU U25	Connected to the management MCU: with a dedicated firmware loaded on the MCU it can be used to switch the SOM on and off from the baseboard

The sequence is: (1) the baseboard applies +5V_BOARD and, once stable, asserts SOM_PWR_EN; (2) the MCU U25 enables the on-board regulators in order (U1 0.85 V core, U5 1.8 V, U10 1.1 V, U12 3.3 V) and checks the PG_0V85 / PG_1V8 / PG_1V1 power-good signals; (3) when all rails are valid the SOM releases SOM_PWR_OK (open-collector goes high through the carrier pull-up); (4) on the assertion of SOM_PWR_OK the supervisor TPS3808G33 automatically asserts the internal reset for 10 ms, guaranteeing a clean reset window while the system becomes stable; (5) only now the baseboard may enable +VCCO_26 / +VCCO_65 and start driving the module I/Os.

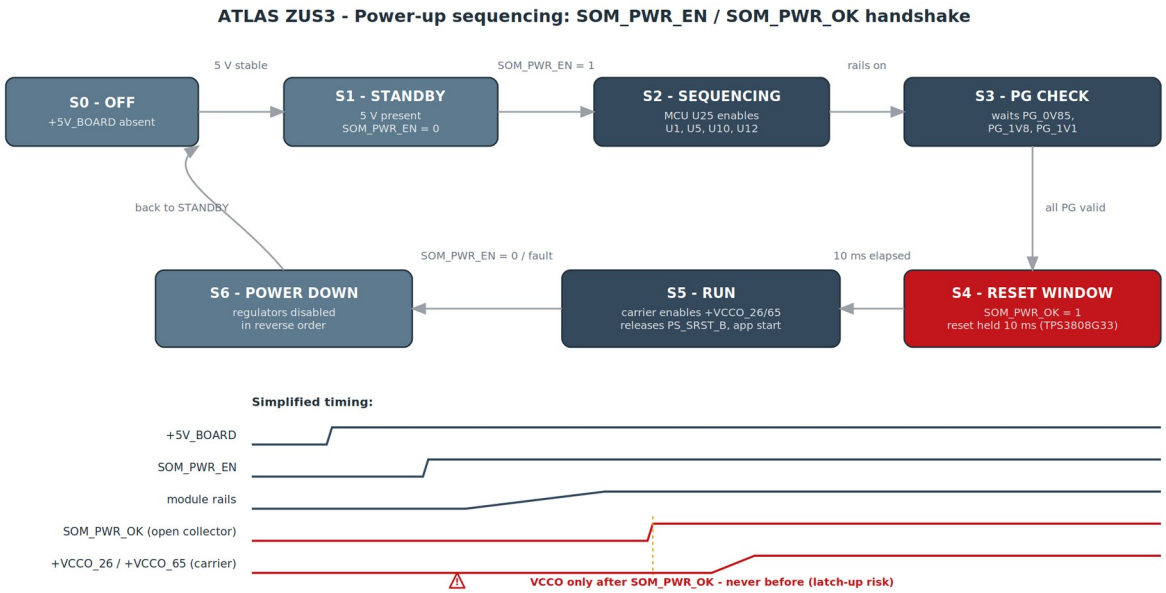

Figure 3 - Power-up sequencing state diagram and simplified timing of the SOM_PWR_EN / SOM_PWR_OK handshake. VCCO is enabled by the carrier only after SOM_PWR_OK.

At power-down the recommended order is the reverse: stop driving I/Os, remove the VCCO rails, deassert SOM_PWR_EN (the MCU disables the regulators in reverse order), then remove the 5 V. SOM_SRSTn (pin 249) remains available to the baseboard as a system reset input at any time during RUN.

Note: The +1V8_PSAUX and +1V8_MCU outputs are service rails: do not exceed 350 mA and 100 mA of external load respectively. The connector has 64 GND pins, distributed between the differential pairs and the I/O groups to guarantee current return and isolation; they are listed in the full table of chapter 7.

4. Clock distribution and MGT section

The main PS reference is oscillator Y1 (DSC1001, 33.3333 MHz) on PS_REF_CLK (ball H14); in the TCL PSU__PSS_REF_CLK__FREQMHZ = 33.333333. Crystal Y2 (32.768 kHz) feeds the PS RTC, kept alive by the +1V5_PSBATT rail when the module is off. A dedicated 25 MHz oscillator Y5 clocks the Ethernet PHY U18.

The references of the four PS-GTR transceivers (bank 505) are generated by the programmable clock generator U15 (Renesas/IDT 5P49V6965, 25 MHz crystal Y3, programmable via I2C0 - address as per the note on sheet 3 of the schematic):

U15 output	Net	Frequency	GTR reference	Use
OUT1	GTR_CLK0_USB_26M_P/N	26 MHz	PS_MGTREFCLK0	USB 3.0 (GT Lane2)
OUT2	GTR_CLK1_DP_27M_P/N	27 MHz	PS_MGTREFCLK1	DisplayPort (GT Lane3) - in the TCL: DP Ref Clk1, 27 MHz
OUT3	GTR_CLK2_SATA_125M_P/N	125 MHz	PS_MGTREFCLK2	SATA (provision; SATA disabled in the project)
OUT4	PCIe_REF_CLK_P/N	100 MHz	- (output on connector, pins 41/43)	PCIe reference for the carrier

The PCIe reference follows the typical SOM scheme: U15 generates the 100 MHz on PCIe_REF_CLK_P/N (connector pins 41/43); the carrier distributes it to the PCIe endpoint and routes it back to the module on pins MGTR_REFCLK3_P/N (35/37), connected to PS_MGTREFCLK3 (E19/E20). In the TCL the PCIe Root Port indeed uses Ref Clk3 at 100 MHz (PSU__PCIE__REF_CLK_SEL = Ref Clk3, PSU__PCIE__REF_CLK_FREQ = 100).

GTR lane	Assignment (TCL)	Connector pins
GT Lane0	PCIe lane 0 (PSU__PCIE__LANE0__IO = GT Lane0)	TX: 58/60 - RX: 52/54
GT Lane1	PCIe lane 1 (PSU__PCIE__LANE1__IO = GT Lane1)	TX: 46/48 - RX: 40/42

GTR lane	Assignment (TCL)	Connector pins
GT Lane2	USB 3.0 (PSU__USB3_0__PERIPHERAL__IO = GT Lane2)	TX: 16/18 - RX: 22/24
GT Lane3	DisplayPort lane 0 (PSU__DISPLAYPORT__LANE0__IO = GT Lane3)	TX: 4/6 - RX: 10/12 (RX unused by DP)

5. Processing System peripherals: MIO assignment and Vivado settings

This chapter lists, for each PS peripheral, the MIO pin assignment (with FPGA ball and bank), the exposure on the SODIMM connector where applicable, and the corresponding settings in the reference Vivado project. Terminology note: the signals listed here are PS MIO (Multiplexed I/O) pins, routed directly from silicon; the term EMIO instead denotes routing of the same peripherals through the Programmable Logic. In the reference project the only EMIO resource used is the 6-bit EMIO GPIO (PSU__GPIO_EMIO__PERIPHERAL__ENABLE = 1, width 6).

5.1 eMMC (SD0 controller)

The eMMC memory U21 (8 GByte) is soldered on the module and connected to the SD0 controller in 8-bit mode. It is the primary boot/storage device of the module.

MIO	Ball	Signal	Function
MIO13	W3	MIO13_MMC_D0	eMMC DATA0
MIO14	W5	MIO14_MMC_D1	eMMC DATA1
MIO15	Y4	MIO15_MMC_D2	eMMC DATA2
MIO16	Y3	MIO16_MMC_D3	eMMC DATA3
MIO17	AA3	MIO17_MMC_D4	eMMC DATA4
MIO18	Y5	MIO18_MMC_D5	eMMC DATA5
MIO19	AA4	MIO19_MMC_D6	eMMC DATA6
MIO20	AB4	MIO20_MMC_D7	eMMC DATA7
MIO21	W6	MIO21_MMC_CMD	eMMC CMD
MIO22	AA6	MIO22_MMC_CLK	eMMC CLK
MIO23	AB5	MIO23_MMC_RST	eMMC RST_N (dedicated reset)

Vivado settings (from the reference TCL):

Vivado parameter	Value
PSU__SD0__PERIPHERAL__ENABLE	1
PSU__SD0__PERIPHERAL__IO	MIO 13 .. 22
PSU__SD0__SLOT_TYPE	eMMC
PSU__SD0__DATA_TRANSFER_MODE	8Bit
PSU__SD0__GRP_CD / GRP_WP / GRP_POW	Disabled (not used for eMMC)
SDIO0 reference clock	200 MHz from IOPLL (actual 187.5 MHz)
PSU__SD0__CLK_200_SDR_OTAP_DLY	0x3
PSU__SD0__CLK_50_DDR_ITAP_DLY / OTAP_DLY	0x12 / 0x6
PSU__SD0__CLK_50_SDR_ITAP_DLY / OTAP_DLY	0x15 / 0x6
MIO electrical configuration	Pull-up, fast slew, 12 mA drive, bank 500 LVCMOS18

5.2 SD Card (SD1 controller)

The SD1 controller is entirely routed to the connector to implement an SD slot on the baseboard: 4-bit bus plus the Card Detect and Write Protect signals.

MIO	Ball	Signal	SODIMM pin	Function
MIO46	C12	MIO46_SD_DATA0	211	SD DATA0
MIO47	B12	MIO47_SD_DATA1	213	SD DATA1
MIO48	A12	MIO48_SD_DATA2	203	SD DATA2
MIO49	D13	MIO49_SD_DATA3	205	SD DATA3
MIO50	A13	MIO50_SD_CMD	207	SD CMD
MIO51	C13	MIO51_SD_CLK	209	SD CLK

MIO	Ball	Signal	SODIMM pin	Function
MIO44	B11	MIO44_SD_WPn	215	Write Protect (active low)
MIO45	A11	MIO45_SD_CDN	217	Card Detect (active low)

Vivado settings:

Vivado parameter	Value
PSU__SD1__PERIPHERAL__ENABLE	1
PSU__SD1__PERIPHERAL__IO	MIO 46 .. 51
PSU__SD1__SLOT_TYPE	SD 2.0
PSU__SD1__DATA_TRANSFER_MODE	4Bit
PSU__SD1__GRP_CD__ENABLE / GRP_WP__ENABLE	0 / 0 (see note below)
SDIO1 reference clock	200 MHz from IOPLL (actual 187.5 MHz)
PSU__SD1__CLK_50_SDR_ITAP_DLY / OTAP_DLY	0x15 / 0x5

Note: The CD/WP groups are disabled in the reference TCL, but the hardware routes MIO44 (WPn) and MIO45 (CDn) to the SODIMM connector: the customer can enable them in Vivado (SD1 - Group CD / Group WP) or handle them as GPIOs. The SD signals are 1.8 V (bank 501): for a 3.3 V SD slot the baseboard must provide level translation.

5.3 Serial ports

PS UART0 (console)

MIO	Ball	Signal	SODIMM pin	Function
MIO10	AA2	MIO10_UART0_RXD	212	UART0 RX (input to the PS)
MIO11	W2	MIO11_UART0_TXD	214	UART0 TX (output from the PS)

Vivado settings:

Vivado parameter	Value
PSU__UART0__PERIPHERAL__ENABLE	1
PSU__UART0__PERIPHERAL__IO	MIO 10 .. 11
PSU__UART0__BAUD_RATE	115200
UART0 reference clock	100 MHz from IOPLL
PSU__UART0__MODEM__ENABLE	0
PSU__UART1__PERIPHERAL__ENABLE	0 (PS UART1 not used)

MCU service UART

Signal	SODIMM pin	Function
MCU_UART1_TX	256	TX from MCU U25 to the baseboard (power log, ADC telemetry, commands)
MCU_UART1_RX	258	MCU RX from the baseboard

This serial port belongs to the management microcontroller, not to the PS: it is available even with the module off (with +5V_BOARD present) and is the diagnostic channel of the power-up sequence. 1.8 V levels referenced to +1V8_MCU.

5.4 QSPI

The QSPI flash U22 (MT25QU512, 512 Mbit, 1.8 V) is soldered on the module on MIO0-5 (bank 500).

MIO	Ball	Signal	Function
MIO0	U4	MIO0_QSPI_SCLK	QSPI SCLK
MIO1	W1	MIO1_QSPI_MISO_Q1	QSPI IO1 / MISO
MIO2	V2	MIO2_QSPI_Q2	QSPI IO2
MIO3	U5	MIO3_QSPI_Q3	QSPI IO3
MIO4	U6	MIO4_QSPI_MOSI_Q0	QSPI IO0 / MOSI
MIO5	AA1	MIO5_QSPI_CSN	QSPI CS_N

In the reference project the QSPI controller is disabled and boot is from eMMC. Settings, and the values to use to enable the flash:

Vivado parameter	Reference project	To enable the flash
PSU__QSPI__PERIPHERAL__ENABLE	0	1
PSU__QSPI__PERIPHERAL__MODE	-	Single
PSU__QSPI__PERIPHERAL__DATA_MODE	-	x4
PSU__QSPI__PERIPHERAL__IO	-	MIO 0 .. 5
PSU__QSPI__GRP_FBCLK__ENABLE	-	0 (no MIO6 routed on the module)
QSPI reference clock	300 MHz from IOPLL	300 MHz from IOPLL

The flash can be used as an alternative boot device by strapping the PS_MODE pins on the carrier (chapter 6).

5.5 USB 2.0 (USB0 + ULPI PHY)

The PS USB0 controller is connected to the USB3320C PHY (U20) through the ULPI bus on MIO52-63 (bank 502); the line side of the PHY (D+/D-, VBUS, ID, CPEN) is exposed on the connector. Crystal Y4 (24 MHz) provides the PHY reference.

MIO	Ball	ULPI signal
MIO52	G14	ULPI CLK (from PHY)
MIO53	F14	ULPI DIR
MIO54	G15	ULPI DATA2
MIO55	C14	ULPI NXT
MIO56	E14	ULPI DATA0
MIO57	B14	ULPI DATA1
MIO58	A14	ULPI STP
MIO59	E15	ULPI DATA3
MIO60	D15	ULPI DATA4
MIO61	G16	ULPI DATA5
MIO62	C15	ULPI DATA6
MIO63	F16	ULPI DATA7

Line-side signal	SODIMM pin	Function
OTG_D_P / OTG_D_N	49 / 47	USB 2.0 data pair (480 Mbit/s)
OTG_VBUS	51	VBUS sense (to divider on the module)
OTG_ID	57	OTG host/device identification
OTG_CPEN	53	VBUS supply enable (to power switch on the carrier)

Vivado settings:

Vivado parameter	Value
PSU__USB0__PERIPHERAL__ENABLE	1
PSU__USB0__PERIPHERAL__IO	MIO 52 .. 63 (ULPI)
PSU__USB0__RESET__ENABLE / __IO	1 / MIO 25 (active low, Separate MIO Pin mode)
PSU__USB3_0__PERIPHERAL__ENABLE	1
PSU__USB3_0__PERIPHERAL__IO	GT Lane2
PSU__USB0__REF_CLK_SEL / __REF_CLK_FREQ	Ref Clk0 / 100 (schematic: 26 MHz from U15 OUT1 - verify consistency)
USB3 bus clock / USB3_DUAL_REF	250 MHz / 20 MHz

For USB 2.0-only use the carrier can ignore the GTR TX2/RX2 lanes.

5.6 LPDDR4

Memory U16 (Nanya NT6AN512T32AV-J2, 16 Gbit, two x16 channels used as a single x32 bus) is connected to the PS DDR bank 504. The ZQ termination uses a 240 ohm resistor (R52/R53); the +1V1_PS_DDR rail powers memory and bank.

Vivado parameter	Value
PSU__DDRC__MEMORY_TYPE	LPDDR 4
PSU__DDRC__SPEED_BIN	LPDDR4_2133
PSU__DDRC__BUS_WIDTH / DRAM_WIDTH	32 Bit / 32 Bits
PSU__DDRC__DEVICE_CAPACITY	16384 MBits (2 GByte)
PSU__CRF_APB__DDR_CTRL__FREQMHZ	533 MHz (actual 526.67 MHz, DPLL source)
PSU__DDRC__ROW_ADDR_COUNT	16
PSU__DDRC__ADDR_MIRROR	1 (mirroring enabled)
PSU__DDRC__ECC	Disabled
PSU__DDRC__DM_DBI	DM_NO_DBI
Training	Data eye, read gate, write leveling enabled
Timing	T_RCD 22, T_RP 20, T_RC 63, T_RAS_MIN 42, T_FAW 40.0
PSU__DDRC__LPDDR4_T_REF_RANGE	Normal (0-85 deg C)

The LPDDR4 is entirely internal to the module: no DDR signal is present on the connector. The memory reset (MPSOC-DDR4-RESETN) and the voltages are managed on board.

5.7 Gigabit Ethernet (GEM3 + KSZ9031RNX)

MIO	Ball	RGMII signal
MIO64	E16	GEM3 TX_CLK
MIO65	B15	GEM3 TXD0
MIO66	D16	GEM3 TXD1
MIO67	G17	GEM3 TXD2
MIO68	B16	GEM3 TXD3
MIO69	A16	GEM3 TX_CTL
MIO70	A17	GEM3 RX_CLK
MIO71	F17	GEM3 RXD0
MIO72	C17	GEM3 RXD1
MIO73	D17	GEM3 RXD2
MIO74	D18	GEM3 RXD3
MIO75	B17	GEM3 RX_CTL
MIO76	F18	GEM MDC
MIO77	B18	GEM MDIO

MDI-side signal	SODIMM pin
ETH_TXA_P/N	5 / 7
ETH_TXB_P/N	11 / 13
ETH_TXC_P/N	17 / 19
ETH_TXD_P/N	23 / 25
ETH_LINK_ON (link LED)	29
ETH_ACTIVITY_B (activity LED)	31
+3V3_ETH (magnetics center-tap)	1

Vivado settings:

Vivado parameter	Value
PSU__ENET3__PERIPHERAL__ENABLE	1
PSU__ENET3__PERIPHERAL__IO	MIO 64 .. 75 (RGMII)
PSU__ENET3__GRP_MDIO__ENABLE / __IO	1 / MDIO 3, MIO 76 .. 77
GEM3 reference clock	125 MHz from IOPLL
PHY MDIO address	0x01 (schematic strap)
PHY 125 MHz clock output	Disabled (schematic strap)
PHY reference clock	Y5, 25 MHz dedicated oscillator
PHY reset / interrupt	MIO24_ETH_RST / MIO7_ETH_INTn (internal to the module)

The carrier only needs the RJ45 connector with magnetics and the LEDs.

5.8 DisplayPort, PCIe, CAN, I2C, GPIO and PMU

DisplayPort

Vivado parameter	Value
PSU__DISPLAYPORT__PERIPHERAL__ENABLE	1
PSU__DISPLAYPORT__LANE0__ENABLE / __IO	1 / GT Lane3 (SODIMM pins 4/6)
PSU__DPAUX__PERIPHERAL__IO	MIO 27 .. 30 (SODIMM pins 32/34/28/30)
PSU__DP__REF_CLK_SEL / __REF_CLK_FREQ	Ref Clk1 / 27 MHz
PSU__DP__LANE_SEL	Single Higher

PCI Express

Vivado parameter	Value
PSU__PCIE__PERIPHERAL__ENABLE / ROOTPORT	1 / Root Port
PSU__PCIE__LANE0__IO / LANE1__IO	GT Lane0 / GT Lane1
PSU__PCIE__LINK_SPEED / MAX_LINK_WIDTH	2.5 Gb/s (Gen1) / x2
PSU__PCIE__RESET__IO	MIO 31 - PERST#, active low (SODIMM pin 59)
PSU__PCIE__REF_CLK_SEL / __REF_CLK_FREQ	Ref Clk3 / 100 MHz (SODIMM pins 35/37)
Class code / Vendor / Device	0x058000 / 0x10EE / 0xD011
BAR0	Memory, 1 MB

CAN

Vivado parameter	Value
PSU__CAN0__PERIPHERAL__ENABLE / __IO	1 / MIO 42 .. 43 (SODIMM pins 204/206)
CAN0/1 reference clock	100 MHz from IOPLL
PSU__CAN1__PERIPHERAL__ENABLE	0 - MIO 8 (CAN1 TX, SODIMM 208) and MIO 9 (CAN1 RX, SODIMM 210) are routed to the connector; enable with CAN1 - IO = MIO 8 .. 9

External CAN transceivers are required on the baseboard.

I2C

Vivado parameter	Value
PSU__I2C0__PERIPHERAL__ENABLE / __IO	1 / MIO 38 .. 39 (SODIMM pins 219/221)
I2C0 bus	On-module: clock generator U15, MAC EEPROM U19; also available to the carrier (mind the occupied addresses)
PSU__I2C1__PERIPHERAL__ENABLE / __IO	1 / MIO 40 .. 41 (SODIMM pins 223/225)
I2C1 bus	Dedicated to the carrier
I2C0/1 reference clock	100 MHz - 1.8 V levels, on-board pull-ups

GPIO and PMU

Vivado parameter	Value
PSU__GPIO0_MIO__PERIPHERAL__ENABLE	1 - MIO12 free GPIO on SODIMM pin 61
PSU__GPIO_EMIO__PERIPHERAL__ENABLE / width	1 / 6 bit towards the PL
PSU__PMU__GPO2..GPO5	MIO 34 .. 37, exposed on SODIMM pins 216-222
PSU__PMU__GPO0/GPO1, PMU_INPUT	MIO 32/33/26 - internal to the module, towards MCU U25

5.9 Other settings of the reference Vivado project

The ZCU-DM-X1-R0 project (Vivado 2022.2, part xczu1eg-sbva484-1-e) contains a block design with: zynq_ultra_ps_e 3.4, a MIPI CSI-2 RX video pipeline (mipi_csi2_rx_subsystem 5.2, demosaic, video processing subsystem, frame buffer write on S_AXI_HPC0_FPD through SmartConnect), two AXI IIC, AXI GPIO, AXI DNA and an interconnect on M_AXI_HPM0_LPD. PL clocks: PL0 150 MHz (IOPLL) and PL1 200 MHz (RPLL); fabric reset enabled; PL-PS interrupts IRQ0/IRQ1 enabled. Main frequencies: APU 1200 MHz (APLL), RPU 500 MHz (IOPLL), DDR 533 MHz (DPLL), DDR interface 266.5 MHz.

6. Baseboard design guidelines

Topic	Guideline
Power	Provide +5V_BOARD on pins 251-259 (5.5 V absolute maximum) with adequate current margin; drive SOM_PWR_EN and wait for SOM_PWR_OK before enabling VCCO and releasing the resets (see 3.5)
PL VCCO	Supply +VCCO_26 (63/64) and +VCCO_65 (101/102) according to the chosen I/O standards, ONLY after SOM_PWR_OK is asserted (latch-up risk); without VCCO the PL banks are unusable
SOM_PWR_OK	Open-collector, active high: provide a pull-up on the carrier and use it as the enable of the VCCO regulators/load switches
Boot mode	PS_MODE0..2 (236/238/240) with pull-up/pull-down straps on the carrier: 000 JTAG, eMMC/SD1/QSPI as per the AMD UG1085 boot mode encoding
JTAG	Chain on pins 224-230 (TCK/TMS/TDI/TDO) plus PS_SRST_B (232); 1.8 V levels
PCIe	Route PCIe_REF_CLK (41/43) to the endpoint and back on MGTR_REFCLK3 (35/37); PERST# from MIO31 (59)
SD card	Provide 1.8 V - 3.3 V level shifters if the slot operates at 3.3 V
Differential pairs	Keep 100 ohm differential impedance and matched lengths for GTR, Ethernet MDI and USB
Service rails	Load +1V8_PSAUX with max 350 mA and +1V8_MCU with max 100 mA
Thermal	Provide heatsinking/airflow so the Zynq UltraScale+ junction temperature never exceeds the AMD maximum rating (100 deg C commercial grade); monitor via SYSMON
RTC	Connect a battery/supercap on +1V5_PSBATT (242) to keep the RTC alive

7. Complete SODIMM connector pinout (260 pins)

The following table lists all the pins of the SODIMM connector. For PL pins it reports the FPGA ball, the pin name according to the AMD pinout (which also encodes the clock capability) and the clock classification; for PS pins (MIO, GTR, JTAG, configuration) it reports ball, bank and FPGA pin name. Category: whether the pin is power, ground, PL I/O, PS MIO, GTR transceiver, JTAG, MCU or other.

Pin	SOM net	Category	Function	FPGA ball	AMD pin name	Bank	Clock
1	+3V3_ETH	Power	3.3 V output for Ethernet magnetics/terminations on the carrier	-	-	-	-
2	GND	GND	Ground	-	-	-	-
3	GND	GND	Ground	-	-	-	-
4	MGTR_TX3_N	PS-GTR	DisplayPort lane 0 (GT Lane3)	A20	PS_MGTRTXN3_505	505 (PS-GTR)	-
5	ETH_TXA_P	Ethernet	MDI pair A+ (KSZ9031RNX PHY)	-	-	-	-
6	MGTR_TX3_P	PS-GTR	DisplayPort lane 0 (GT Lane3)	A19	PS_MGTRTXP3_505	505 (PS-GTR)	-
7	ETH_TXA_N	Ethernet	MDI pair A-	-	-	-	-
8	GND	GND	Ground	-	-	-	-
9	GND	GND	Ground	-	-	-	-
10	MGTR_RX3_N	PS-GTR	GT Lane3 RX (unused by DP)	B22	PS_MGTRRXN3_505	505 (PS-GTR)	-
11	ETH_TXB_P	Ethernet	MDI pair B+	-	-	-	-
12	MGTR_RX3_P	PS-GTR	GT Lane3 RX (unused by DP)	B21	PS_MGTRRXP3_505	505 (PS-GTR)	-
13	ETH_TXB_N	Ethernet	MDI pair B-	-	-	-	-
14	GND	GND	Ground	-	-	-	-
15	GND	GND	Ground	-	-	-	-
16	MGTR_TX2_N	PS-GTR	USB 3.0 TX (GT Lane2)	C20	PS_MGTRTXN2_505	505 (PS-GTR)	-
17	ETH_TXC_P	Ethernet	MDI pair C+	-	-	-	-
18	MGTR_TX2_P	PS-GTR	USB 3.0 TX (GT Lane2)	C19	PS_MGTRTXP2_505	505 (PS-GTR)	-
19	ETH_TXC_N	Ethernet	MDI pair C-	-	-	-	-
20	GND	GND	Ground	-	-	-	-
21	GND	GND	Ground	-	-	-	-
22	MGTR_RX2_N	PS-GTR	USB 3.0 RX (GT Lane2)	D22	PS_MGTRRXN2_505	505 (PS-GTR)	-
23	ETH_TXD_P	Ethernet	MDI pair D+	-	-	-	-
24	MGTR_RX2_P	PS-GTR	USB 3.0 RX (GT Lane2)	D21	PS_MGTRRXP2_505	505 (PS-GTR)	-
25	ETH_TXD_N	Ethernet	MDI pair D-	-	-	-	-
26	GND	GND	Ground	-	-	-	-
27	GND	GND	Ground	-	-	-	-

Pin	SOM net	Category	Function	FPGA ball	AMD pin name	Bank	Clock
28	MIO29_DP_OE	PS-MIO	DP OE	F9	PS_MIO29	501 (VCCO_PSIO1, 1.8 V)	-
29	ETH_LINK_ON	Ethernet	Link LED	-	-	-	-
30	MIO30_DP_AUX_IN	PS-MIO	DP AUX IN	G10	PS_MIO30	501 (VCCO_PSIO1, 1.8 V)	-
31	ETH_ACTIVITY_B	Ethernet	Activity LED (active low)	-	-	-	-
32	MIO27_DP_AUX_OUT	PS-MIO	DP AUX OUT	G11	PS_MIO27	501 (VCCO_PSIO1, 1.8 V)	-
33	GND	GND	Ground	-	-	-	-
34	MIO28_DP_HPD	PS-MIO	DP HPD	G12	PS_MIO28	501 (VCCO_PSIO1, 1.8 V)	-
35	MGTR_REFCLK3_N	PS-GTR	GT reference clock #3 - 100 MHz PCIe (input from carrier)	E20	PS_MGTREFCLK3N_505	505 (PS-GTR)	-
36	+1V8_PSAUX	Power	1.8 V auxiliary output (MIO level reference / low-power carrier use)	-	-	-	-
37	MGTR_REFCLK3_P	PS-GTR	GT reference clock #3 - 100 MHz PCIe (input from carrier)	E19	PS_MGTREFCLK3P_505	505 (PS-GTR)	-
38	GND	GND	Ground	-	-	-	-
39	GND	GND	Ground	-	-	-	-
40	MGTR_RX1_N	PS-GTR	PCIe lane 1 RX (GT Lane1)	H22	PS_MGTRRXN1_505	505 (PS-GTR)	-
41	PCIe_REF_CLK_N	Clock	100 MHz PCIe reference clock output generated by U15 (OUT4); the carrier routes it to the endpoint and/or back to MGTR_REFCLK3	-	-	-	-
42	MGTR_RX1_P	PS-GTR	PCIe lane 1 RX (GT Lane1)	H21	PS_MGTRRXP1_505	505 (PS-GTR)	-
43	PCIe_REF_CLK_P	Clock	100 MHz PCIe reference clock output generated by U15 (OUT4); the carrier routes it to the endpoint and/or back to MGTR_REFCLK3	-	-	-	-
44	GND	GND	Ground	-	-	-	-
45	GND	GND	Ground	-	-	-	-
46	MGTR_TX1_N	PS-GTR	PCIe lane 1 TX (GT Lane1)	F22	PS_MGTRTXN1_505	505 (PS-GTR)	-
47	OTG_D_N	USB 2.0	USB 2.0 D- (USB3320C PHY)	-	-	-	-
48	MGTR_TX1_P	PS-GTR	PCIe lane 1 TX (GT Lane1)	F21	PS_MGTRTXP1_505	505 (PS-GTR)	-
49	OTG_D_P	USB 2.0	USB 2.0 D+ (USB3320C PHY)	-	-	-	-
50	GND	GND	Ground	-	-	-	-
51	OTG_VBUS	USB 2.0	USB VBUS sense	-	-	-	-
52	MGTR_RX0_N	PS-GTR	PCIe lane 0 RX (GT Lane0)	M22	PS_MGTRRXN0_505	505 (PS-GTR)	-
53	OTG_CPEN	USB 2.0	VBUS charge-pump enable	-	-	-	-
54	MGTR_RX0_P	PS-GTR	PCIe lane 0 RX (GT Lane0)	M21	PS_MGTRRXP0_505	505 (PS-GTR)	-
55	GND	GND	Ground	-	-	-	-
56	GND	GND	Ground	-	-	-	-
57	OTG_ID	USB 2.0	USB OTG ID	-	-	-	-
58	MGTR_TX0_N	PS-GTR	PCIe lane 0 TX (GT Lane0)	K22	PS_MGTRTXN0_505	505 (PS-GTR)	-
59	MIO31_PCIe_RSTn	PS-MIO	PCIe RESET_N	F11	PS_MIO31	501 (VCCO_PSIO1, 1.8 V)	-
60	MGTR_TX0_P	PS-GTR	PCIe lane 0 TX (GT Lane0)	K21	PS_MGTRTXP0_505	505 (PS-GTR)	-
61	MIO12_GPIO	PS-MIO	GPIO	AB2	PS_MIO12	500 (VCCO_PSIO0, 1.8 V)	-
62	GND	GND	Ground	-	-	-	-
63	+VCCO_26	Power	PL bank 26 VCCO input (from carrier: 1.2-3.3 V, sets the HD bank I/O standard)	-	-	-	-
64	+VCCO_26	Power	PL bank 26 VCCO input (from carrier: 1.2-3.3 V, sets the HD bank I/O standard)	-	-	-	-
65	IO26_L11P	PL	PL I/O, bank 26	B6	IO_L11P_AD1P_26	26	I/O standard
66	IO26_L12P	PL	PL I/O, bank 26	B7	IO_L12P_AD0P_26	26	I/O standard
67	IO26_L11N	PL	PL I/O, bank 26	B5	IO_L11N_AD1N_26	26	I/O standard
68	IO26_L12N	PL	PL I/O, bank 26	A6	IO_L12N_AD0N_26	26	I/O standard
69	GND	GND	Ground	-	-	-	-
70	GND	GND	Ground	-	-	-	-
71	IO26_L9P	PL	PL I/O, bank 26	B9	IO_L9P_AD3P_26	26	I/O

Pin	SOM net	Category	Function	FPGA ball	AMD pin name	Bank	Clock
							standard
72	IO26_L10P	PL	PL I/O, bank 26	A8	IO_L10P_AD2P_26	26	I/O standard
73	IO26_L9N	PL	PL I/O, bank 26	A9	IO_L9N_AD3N_26	26	I/O standard
74	IO26_L10N	PL	PL I/O, bank 26	A7	IO_L10N_AD2N_26	26	I/O standard
75	GND	GND	Ground	-	-	-	-
76	GND	GND	Ground	-	-	-	-
77	IO26_L7P	PL	PL I/O, bank 26	D5	IO_L7P_HDGC_AD5P_26	26	HDGC (HD Global Clock)
78	IO26_L8P	PL	PL I/O, bank 26	C8	IO_L8P_HDGC_AD4P_26	26	HDGC (HD Global Clock)
79	IO26_L7N	PL	PL I/O, bank 26	C5	IO_L7N_HDGC_AD5N_26	26	HDGC (HD Global Clock)
80	IO26_L8N	PL	PL I/O, bank 26	C7	IO_L8N_HDGC_AD4N_26	26	HDGC (HD Global Clock)
81	GND	GND	Ground	-	-	-	-
82	GND	GND	Ground	-	-	-	-
83	IO26_L5P	PL	PL I/O, bank 26	D7	IO_L5P_HDGC_AD7P_26	26	HDGC (HD Global Clock)
84	IO26_L6P	PL	PL I/O, bank 26	E8	IO_L6P_HDGC_AD6P_26	26	HDGC (HD Global Clock)
85	IO26_L5N	PL	PL I/O, bank 26	D6	IO_L5N_HDGC_AD7N_26	26	HDGC (HD Global Clock)
86	IO26_L6N	PL	PL I/O, bank 26	D8	IO_L6N_HDGC_AD6N_26	26	HDGC (HD Global Clock)
87	GND	GND	Ground	-	-	-	-
88	GND	GND	Ground	-	-	-	-
89	IO26_L3P	PL	PL I/O, bank 26	E6	IO_L3P_AD9P_26	26	I/O standard
90	IO26_L4P	PL	PL I/O, bank 26	F8	IO_L4P_AD8P_26	26	I/O standard
91	IO26_L3N	PL	PL I/O, bank 26	E5	IO_L3N_AD9N_26	26	I/O standard
92	IO26_L4N	PL	PL I/O, bank 26	F7	IO_L4N_AD8N_26	26	I/O standard
93	GND	GND	Ground	-	-	-	-
94	GND	GND	Ground	-	-	-	-
95	IO26_L1P	PL	PL I/O, bank 26	G6	IO_L1P_AD11P_26	26	I/O standard
96	IO26_L2P	PL	PL I/O, bank 26	G7	IO_L2P_AD10P_26	26	I/O standard
97	IO26_L1N	PL	PL I/O, bank 26	G5	IO_L1N_AD11N_26	26	I/O standard
98	IO26_L2N	PL	PL I/O, bank 26	F6	IO_L2N_AD10N_26	26	I/O standard
99	GND	GND	Ground	-	-	-	-
100	GND	GND	Ground	-	-	-	-
101	+VCCO_65	Power	PL bank 65 VCCO input (from carrier: 1.0-1.8 V, HP bank)	-	-	-	-
102	+VCCO_65	Power	PL bank 65 VCCO input (from carrier: 1.0-1.8 V, HP bank)	-	-	-	-
103	NC	NC	Not connected (reserved)	-	-	-	-
104	IO66_T0U_N12_VRP	PL	PL I/O, bank 66	B4	IO_T0U_N12_VRP_66	66	VRP (DCI calibration)
105	IO66_T3U_N12	PL	PL I/O, bank 66	A2	IO_T3U_N12_66	66	I/O standard

Pin	SOM net	Category	Function	FPGA ball	AMD pin name	Bank	Clock
106	IO66_VREF	PL	PL I/O, bank 66	C4	VREF_66	66	Bank VREF
107	GND	GND	Ground	-	-	-	-
108	GND	GND	Ground	-	-	-	-
109	IO66_L11P	PL	PL I/O, bank 66	B2	IO_L11P_T1U_N8_GC_66	66	GC (Global Clock)
110	IO66_L12P	PL	PL I/O, bank 66	A4	IO_L12P_T1U_N10_GC_66	66	GC (Global Clock)
111	IO66_L11N	PL	PL I/O, bank 66	B1	IO_L11N_T1U_N9_GC_66	66	GC (Global Clock)
112	IO66_L12N	PL	PL I/O, bank 66	A3	IO_L12N_T1U_N11_GC_66	66	GC (Global Clock)
113	GND	GND	Ground	-	-	-	-
114	GND	GND	Ground	-	-	-	-
115	IO65_T1U	PL	PL I/O, bank 65	N3	IO_T1U_N12_65	65	I/O standard
116	IO65_T3U	PL	PL I/O, bank 65	F4	IO_T3U_N12_65	65	I/O standard
117	IO65_VREF	PL	PL I/O, bank 65	K5	VREF_65	65	Bank VREF
118	IO65_T2U	PL	PL I/O, bank 65	H3	IO_T2U_N12_65	65	I/O standard
119	GND	GND	Ground	-	-	-	-
120	GND	GND	Ground	-	-	-	-
121	IO65_L21P	PL	PL I/O, bank 65	E1	IO_L21P_T3L_N4_AD8P_65	65	I/O standard
122	IO65_L24P	PL	PL I/O, bank 65	D2	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	65	I/O standard
123	IO65_L21N	PL	PL I/O, bank 65	D1	IO_L21N_T3L_N5_AD8N_65	65	I/O standard
124	IO65_L24N	PL	PL I/O, bank 65	C2	IO_L24N_T3U_N11_PERSTN0_65	65	I/O standard
125	GND	GND	Ground	-	-	-	-
126	GND	GND	Ground	-	-	-	-
127	IO65_L23P	PL	PL I/O, bank 65	F3	IO_L23P_T3U_N8_I2C_SCLK_65	65	I/O standard
128	IO65_L22P	PL	PL I/O, bank 65	D3	IO_L22P_T3U_N6_DBC_AD0P_65	65	DBC (Dual Byte Clock)
129	IO65_L23N	PL	PL I/O, bank 65	F2	IO_L23N_T3U_N9_65	65	I/O standard
130	IO65_L22N	PL	PL I/O, bank 65	C3	IO_L22N_T3U_N7_DBC_AD0N_65	65	DBC (Dual Byte Clock)
131	GND	GND	Ground	-	-	-	-
132	GND	GND	Ground	-	-	-	-
133	IO65_L19P	PL	PL I/O, bank 65	G1	IO_L19P_T3L_N0_DBC_AD9P_65	65	DBC (Dual Byte Clock)
134	IO65_L20P	PL	PL I/O, bank 65	E4	IO_L20P_T3L_N2_AD1P_65	65	I/O standard
135	IO65_L19N	PL	PL I/O, bank 65	F1	IO_L19N_T3L_N1_DBC_AD9N_65	65	DBC (Dual Byte Clock)
136	IO65_L20N	PL	PL I/O, bank 65	E3	IO_L20N_T3L_N3_AD1N_65	65	I/O standard
137	GND	GND	Ground	-	-	-	-
138	GND	GND	Ground	-	-	-	-
139	IO65_L17P	PL	PL I/O, bank 65	H2	IO_L17P_T2U_N8_AD10P_65	65	I/O standard
140	IO65_L18P	PL	PL I/O, bank 65	H4	IO_L18P_T2U_N10_AD2P_65	65	I/O standard
141	IO65_L17N	PL	PL I/O, bank 65	G2	IO_L17N_T2U_N9_AD10N_65	65	I/O standard
142	IO65_L18N	PL	PL I/O, bank 65	G4	IO_L18N_T2U_N11_AD2N_65	65	I/O standard
143	GND	GND	Ground	-	-	-	-

Pin	SOM net	Category	Function	FPGA ball	AMD pin name	Bank	Clock
144	GND	GND	Ground	-	-	-	-
145	GND	GND	Ground	-	-	-	-
146	GND	GND	Ground	-	-	-	-
147	IO65_L13P	PL	PL I/O, bank 65	J3	IO_L13P_T2L_N0_GC_QBC_65	65	GC (Global Clock), QBC (Quad Byte Clock)
148	IO65_L16P	PL	PL I/O, bank 65	J5	IO_L16P_T2U_N6_QBC_AD3P_65	65	QBC (Quad Byte Clock)
149	IO65_L13N	PL	PL I/O, bank 65	J2	IO_L13N_T2L_N1_GC_QBC_65	65	GC (Global Clock), QBC (Quad Byte Clock)
150	IO65_L16N	PL	PL I/O, bank 65	H5	IO_L16N_T2U_N7_QBC_AD3N_65	65	QBC (Quad Byte Clock)
151	GND	GND	Ground	-	-	-	-
152	GND	GND	Ground	-	-	-	-
153	IO65_L15P	PL	PL I/O, bank 65	K1	IO_L15P_T2L_N4_AD11P_65	65	I/O standard
154	IO65_L14P	PL	PL I/O, bank 65	K4	IO_L14P_T2L_N2_GC_65	65	GC (Global Clock)
155	IO65_L15N	PL	PL I/O, bank 65	J1	IO_L15N_T2L_N5_AD11N_65	65	I/O standard
156	IO65_L14N	PL	PL I/O, bank 65	K3	IO_L14N_T2L_N3_GC_65	65	GC (Global Clock)
157	GND	GND	Ground	-	-	-	-
158	GND	GND	Ground	-	-	-	-
159	IO65_L11P	PL	PL I/O, bank 65	L2	IO_L11P_T1U_N8_GC_65	65	GC (Global Clock)
160	IO65_L12P	PL	PL I/O, bank 65	L4	IO_L12P_T1U_N10_GC_65	65	GC (Global Clock)
161	IO65_L11N	PL	PL I/O, bank 65	L1	IO_L11N_T1U_N9_GC_65	65	GC (Global Clock)
162	IO65_L12N	PL	PL I/O, bank 65	L3	IO_L12N_T1U_N11_GC_65	65	GC (Global Clock)
163	GND	GND	Ground	-	-	-	-
164	GND	GND	Ground	-	-	-	-
165	IO65_L09P	PL	PL I/O, bank 65	M2	IO_L9P_T1L_N4_AD12P_65	65	I/O standard
166	IO65_L10P	PL	PL I/O, bank 65	M5	IO_L10P_T1U_N6_QBC_AD4P_65	65	QBC (Quad Byte Clock)
167	IO65_L09N	PL	PL I/O, bank 65	M1	IO_L9N_T1L_N5_AD12N_65	65	I/O standard
168	IO65_L10N	PL	PL I/O, bank 65	M4	IO_L10N_T1U_N7_QBC_AD4N_65	65	QBC (Quad Byte Clock)
169	GND	GND	Ground	-	-	-	-
170	GND	GND	Ground	-	-	-	-
171	IO65_L07P	PL	PL I/O, bank 65	N2	IO_L7P_T1L_N0_QBC_AD13P_65	65	QBC (Quad Byte Clock)
172	IO65_L08P	PL	PL I/O, bank 65	N5	IO_L8P_T1L_N2_AD5P_65	65	I/O standard
173	IO65_L07N	PL	PL I/O, bank 65	P1	IO_L7N_T1L_N1_QBC_AD13N_65	65	QBC (Quad

Pin	SOM net	Category	Function	FPGA ball	AMD pin name	Bank	Clock
							Byte Clock)
174	IO65_L08N	PL	PL I/O, bank 65	N4	IO_L8N_T1L_N3_AD5N_65	65	I/O standard
175	GND	GND	Ground	-	-	-	-
176	GND	GND	Ground	-	-	-	-
177	IO65_L06P	PL	PL I/O, bank 65	P5	IO_L6P_T0U_N10_AD6P_65	65	I/O standard
178	IO65_L05P	PL	PL I/O, bank 65	R1	IO_L5P_T0U_N8_AD14P_65	65	I/O standard
179	IO65_L06N	PL	PL I/O, bank 65	R5	IO_L6N_T0U_N11_AD6N_65	65	I/O standard
180	IO65_L05N	PL	PL I/O, bank 65	T1	IO_L5N_T0U_N9_AD14N_65	65	I/O standard
181	GND	GND	Ground	-	-	-	-
182	GND	GND	Ground	-	-	-	-
183	IO65_L02P	PL	PL I/O, bank 65	P3	IO_L2P_T0L_N2_65	65	I/O standard
184	IO65_L01P	PL	PL I/O, bank 65	T3	IO_L1P_T0L_N0_DBC_65	65	DBC (Dual Byte Clock)
185	IO65_L02N	PL	PL I/O, bank 65	R3	IO_L2N_T0L_N3_65	65	I/O standard
186	IO65_L01N	PL	PL I/O, bank 65	T2	IO_L1N_T0L_N1_DBC_65	65	DBC (Dual Byte Clock)
187	GND	GND	Ground	-	-	-	-
188	GND	GND	Ground	-	-	-	-
189	IO65_L04P	PL	PL I/O, bank 65	R4	IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	65	DBC (Dual Byte Clock)
190	IO65_L03P	PL	PL I/O, bank 65	U2	IO_L3P_T0L_N4_AD15P_65	65	I/O standard
191	IO65_L04N	PL	PL I/O, bank 65	T4	IO_L4N_T0U_N7_DBC_AD7N_65	65	DBC (Dual Byte Clock)
192	IO65_L03N	PL	PL I/O, bank 65	U1	IO_L3N_T0L_N5_AD15N_65	65	I/O standard
193	GND	GND	Ground	-	-	-	-
194	GND	GND	Ground	-	-	-	-
195	NC	NC	Not connected (reserved)	-	-	-	-
196	NC	NC	Not connected (reserved)	-	-	-	-
197	NC	NC	Not connected (reserved)	-	-	-	-
198	NC	NC	Not connected (reserved)	-	-	-	-
199	NC	NC	Not connected (reserved)	-	-	-	-
200	NC	NC	Not connected (reserved)	-	-	-	-
201	+1V8_PSAUX	Power	1.8 V auxiliary output (MIO level reference / low-power carrier use)	-	-	-	-
202	+1V8_PSAUX	Power	1.8 V auxiliary output (MIO level reference / low-power carrier use)	-	-	-	-
203	MIO48_SD_DATA2	PS-MIO	SD1 DATA2	A12	PS_MIO48	501 (VCCO_PSIO1, 1.8 V)	-
204	MIO42_CAN0_RX	PS-MIO	CAN0 RX	D12	PS_MIO42	501 (VCCO_PSIO1, 1.8 V)	-
205	MIO49_SD_DATA3	PS-MIO	SD1 DATA3	D13	PS_MIO49	501 (VCCO_PSIO1, 1.8 V)	-
206	MIO43_CAN0_TX	PS-MIO	CAN0 TX	E13	PS_MIO43	501 (VCCO_PSIO1, 1.8 V)	-
207	MIO50_SD_CMD	PS-MIO	SD1 CMD	A13	PS_MIO50	501 (VCCO_PSIO1, 1.8 V)	-
208	MIO8_CAN1_TX	PS-MIO	CAN1 TX	V3	PS_MIO8	500 (VCCO_PSIO0, 1.8 V)	-
209	MIO51_SD_CLK	PS-MIO	SD1 CLK	C13	PS_MIO51	501 (VCCO_PSIO1, 1.8 V)	-

Pin	SOM net	Category	Function	FPGA ball	AMD pin name	Bank	Clock
210	MIO9_CAN1_RX	PS-MIO	CAN1 RX	V5	PS_MIO9	500 (VCCO_PSIO0, 1.8 V)	-
211	MIO46_SD_DATA0	PS-MIO	SD1 DATA0	C12	PS_MIO46	501 (VCCO_PSIO1, 1.8 V)	-
212	MIO10_UART0_RXD	PS-MIO	UART0 RXD	AA2	PS_MIO10	500 (VCCO_PSIO0, 1.8 V)	-
213	MIO47_SD_DATA1	PS-MIO	SD1 DATA1	B12	PS_MIO47	501 (VCCO_PSIO1, 1.8 V)	-
214	MIO11_UART0_TXD	PS-MIO	UART0 TXD	W2	PS_MIO11	500 (VCCO_PSIO0, 1.8 V)	-
215	MIO44_SD_WPn	PS-MIO	SD1 WPn	B11	PS_MIO44	501 (VCCO_PSIO1, 1.8 V)	-
216	MIO34_PMU_GPO2	PS-MIO	PMU GPO2	F13	PS_MIO34	501 (VCCO_PSIO1, 1.8 V)	-
217	MIO45_SD_CDN	PS-MIO	SD1 CDn	A11	PS_MIO45	501 (VCCO_PSIO1, 1.8 V)	-
218	MIO35_PMU_GPO3	PS-MIO	PMU GPO3	E10	PS_MIO35	501 (VCCO_PSIO1, 1.8 V)	-
219	MIO38_I2C0_SCL	PS-MIO	I2C0 SCL	C9	PS_MIO38	501 (VCCO_PSIO1, 1.8 V)	-
220	MIO36_PMU_GPO4	PS-MIO	PMU GPO4	D10	PS_MIO36	501 (VCCO_PSIO1, 1.8 V)	-
221	MIO39_I2C0_SDA	PS-MIO	I2C0 SDA	C10	PS_MIO39	501 (VCCO_PSIO1, 1.8 V)	-
222	MIO37_PMU_GPO5	PS-MIO	PMU GPO5	E11	PS_MIO37	501 (VCCO_PSIO1, 1.8 V)	-
223	MIO40_I2C1_SCL	PS-MIO	I2C1 SCL	D11	PS_MIO40	501 (VCCO_PSIO1, 1.8 V)	-
224	JTAG_TCK	JTAG	PS/PL JTAG chain	H13	PS_JTAG_TCK	503 (VCCO_PSIO3, 1.8 V)	-
225	MIO41_I2C1_SDA	PS-MIO	I2C1 SDA	B10	PS_MIO41	501 (VCCO_PSIO1, 1.8 V)	-
226	JTAG_TMS	JTAG	PS/PL JTAG chain	J12	PS_JTAG_TMS	503 (VCCO_PSIO3, 1.8 V)	-
227	NC	NC	Not connected (reserved)	-	-	-	-
228	JTAG_TDI	JTAG	PS/PL JTAG chain	H12	PS_JTAG_TDI	503 (VCCO_PSIO3, 1.8 V)	-
229	NC	NC	Not connected (reserved)	-	-	-	-
230	JTAG_TDO	JTAG	PS/PL JTAG chain	J13	PS_JTAG_TDO	503 (VCCO_PSIO3, 1.8 V)	-
231	NC	NC	Not connected (reserved)	-	-	-	-
232	PS_SRST_B	PS config	PS system reset (active low)	K13	PS_SRST_B	503 (VCCO_PSIO3, 1.8 V)	-
233	NC	NC	Not connected (reserved)	-	-	-	-
234	GND	GND	Ground	-	-	-	-
235	NC	NC	Not connected (reserved)	-	-	-	-
236	PS_MODE0	PS config	Boot mode bit 0	J16	PS_MODE0	503 (VCCO_PSIO3, 1.8 V)	-
237	NC	NC	Not connected (reserved)	-	-	-	-
238	PS_MODE1	PS config	Boot mode bit 1	H15	PS_MODE1	503 (VCCO_PSIO3, 1.8 V)	-
239	ADC_V_P	Analog	SYSMON differential analog input (0-1 V)	L10	VP	SYSMON (dedicato)	-

Pin	SOM net	Category	Function	FPGA ball	AMD pin name	Bank	Clock
240	PS_MODE2	PS config	Boot mode bit 2	J15	PS_MODE2	503 (VCCO_PSIO3, 1.8 V)	-
241	ADC_V_N	Analog	SYSMON differential analog input (0-1 V)	M9	VN	SYSMON (dedicato)	-
242	+1V5_PSBATT	Power	PS RTC battery input (VCC_PSBATT)	-	-	-	-
243	SOM_PWR_EN	Power control	Module power-enable input (to MCU U25)	-	-	-	-
244	NC	NC	Not connected (reserved)	-	-	-	-
245	SOM_PWR_ON	Power control	Power-up handshake (MCU U25)	-	-	-	-
246	NC	NC	Not connected (reserved)	-	-	-	-
247	SOM_PWR_OK	Power control	Overall module power-good output	-	-	-	-
248	NC	NC	Not connected (reserved)	-	-	-	-
249	SOM_SRSTn	Power control	Module system reset (active low)	-	-	-	-
250	MCU_RSTn	MCU	MCU reset (active low)	-	-	-	-
251	+5V_BOARD	Power	Main module supply input (5 V)	-	-	-	-
252	SWDIO	MCU	MCU SWD debug data	-	-	-	-
253	+5V_BOARD	Power	Main module supply input (5 V)	-	-	-	-
254	SWCLK	MCU	MCU SWD debug clock	-	-	-	-
255	+5V_BOARD	Power	Main module supply input (5 V)	-	-	-	-
256	MCU_UART1_TX	MCU	MCU service UART (TX to carrier)	-	-	-	-
257	+5V_BOARD	Power	Main module supply input (5 V)	-	-	-	-
258	MCU_UART1_RX	MCU	MCU service UART (RX from carrier)	-	-	-	-
259	+5V_BOARD	Power	Main module supply input (5 V)	-	-	-	-
260	+1V8_MCU	Power	1.8 V MCU output (level reference for MCU signals)	-	-	-	-