HARDWARE DEVELOPMENT PLATFORM · FPGA + AI

ZU-NEXUS-AI

Advanced AI Vision for Embedded Systems

The strategic nexus between multiprocessor FPGA technology and AI acceleration

MEDICAL | RAILWAY | INDUSTRIAL | DRONES / UAV

The ZU-NEXUS-AI Platform

The nexus between multi processor FPGA and neural acceleration

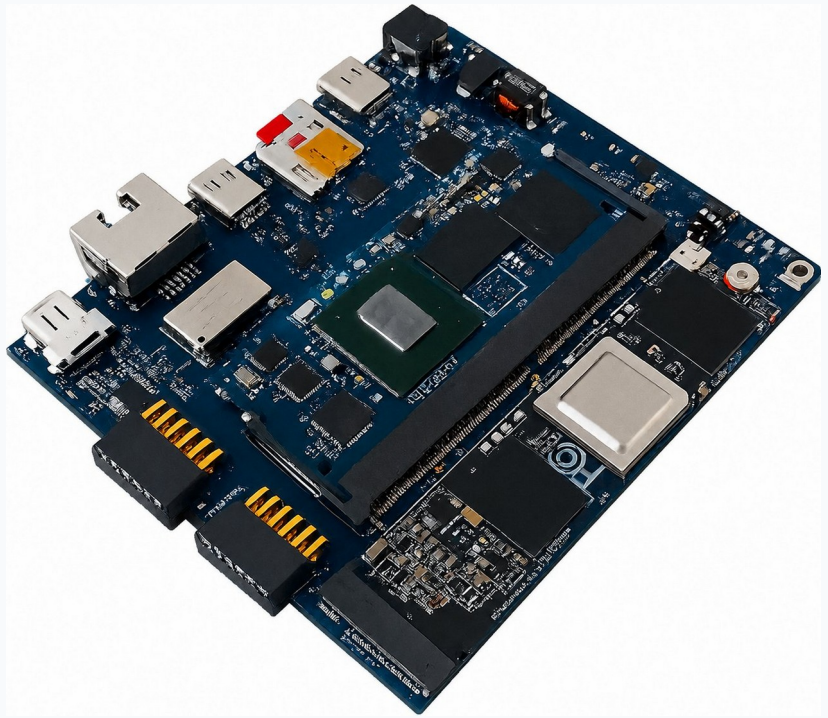
NEXUS = STRATEGIC CONNECTION

A highly flexible and high-performance hardware development platform combining the Zynq UltraScale+ multiprocessor SoC with a dedicated neural accelerator.

25 TOPS
Peak INT8 neural acceleration

4 Quad Arm Cortex-A53

154 K logic cell on ZU3EG

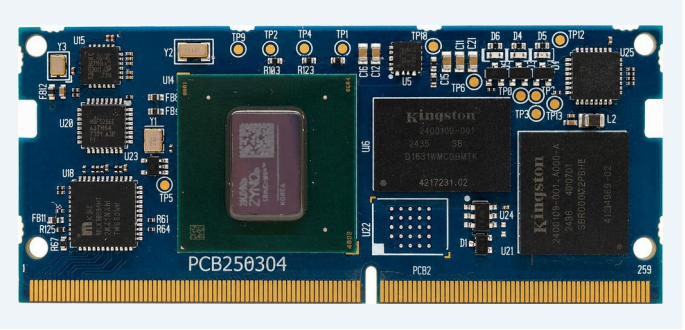


ZU-NEXUS-AI Board — SOM Zynq UltraScale+ + NPU accelerator module on M.2 PCIe

- ✓ 3 MIPI camera expansion
- ✓ PCIe Gen2/3
- ✓ Ethernet · USB · DisplayPort
- ✓ Compact SWaP form factor

Platform Architecture

Three hardware components integrated on the ZU-NEXUS-AI board



SOM Zynq UltraScale+

Zynq MPSoC · SoDIMM4

- → SOC: ZU1EG / ZU2EG / ZU3EG
- → APU: 4× ARM Cortex-A53 @ 1.2 GHz
- → RPU: 2× ARM Cortex-R5 (lockstep)
- → RAM: 2Gbyte LPDDR4 32-bit
- → Storage: 8 Gbyte eMMC + QSPI Flash
- → I/F: 4× MGT (PCIe / USB3 / DP)
- → Power: 5V in / 0.85–3.3V out
- → Clock: 5P49V6965 synth

ZU-NEXUS-AI Board

Carrier Board

- → USB-C Dual-Role (USB 3.0)
- → USB-C JTAG/Console (FTDI)
- → DisplayPort (DP 1.x)
- → Ethernet GbE (RGMII)
- → SD Card
- → M.2 PCIe Key-M ×2 lane
- → MIPI CSI-2 ZIF 22-pin up 2 Mipi Cameras
- → Exp. Connectors (Standard SYZYGY)

DX-M1
M.2 2280

DX-M1M
M.2 2242

NPU Accelerator Module

DeepX DX-M1 / DX-M1M

- → NPU: DX-M1 8-core · 25 TOPS
- → Interface: PCIe Gen2 ×2
- → Two M.2 Key-M form factors:
- → M.2 2280 Key-M (DX-M1)
- → M.2 2242 Key-M (DX-M1M)
- → Power: TDP < 5 W

Multi-sector Applications

A versatile AI vision platform for high-value domains

01

Medical

Diagnostic imaging

Real-time processing of ultrasound images, enhancement, anatomical structure detection and diagnosis support.

Ultrasound · endoscopy · imaging

02

Railway

Sensor fusion

Fusion of camera vision with radar systems for obstacle detection, infrastructure monitoring and track safety.

Camera + radar · ATO · inspection

03

Industrial

Process control

Automated visual inspection on the production line, quality control, defect detection and real-time robot guidance.

Quality control · machine vision

04

Drones / UAV

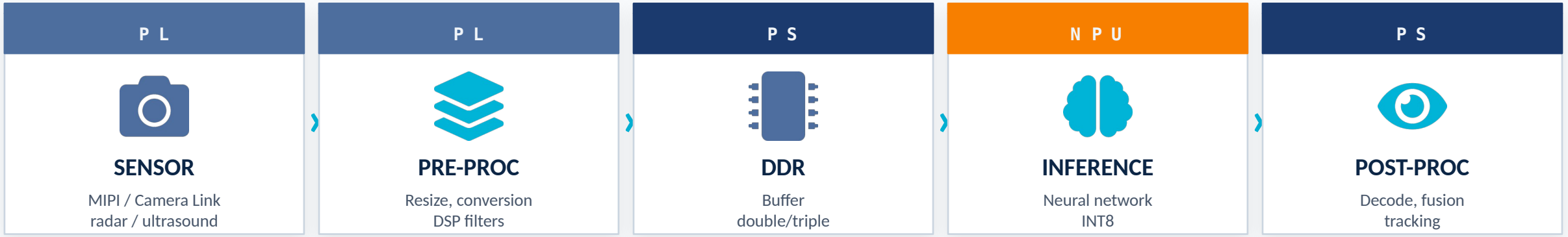
Aerial vision

On-board detection and tracking, obstacle avoidance, mapping and reconnaissance with low-power EO/IR payload (SWaP).

Detection · ISR · mapping

The Processing Pipeline

Optimal workload distribution across FPGA, CPU and neural accelerator



PL *FPGA fabric Zynq US+* · ***PS*** *Linux on Cortex-A53* · ***NPU*** *M.2 neural accelerator module*

WHY THIS ARCHITECTURE

Deterministic pre-processing

The FPGA handles acquisition and conversion at fixed, clock-cycle-accurate latency.

Offloaded CPU

Heavy image operations do not burden ARM cores, which remain free for application logic.

Dedicated NPU

The accelerator runs almost exclusively pure inference, maintaining high and constant throughput.

Multi-sensor fusion

Post-processing fuses camera, radar and other sensors into a single coherent stream.

KED Added Value

Embedded engineering expertise to customize the platform

Linux BSP & Custom Operating Systems

- Complete Board Support Package for the Zynq UltraScale+ platform
- Custom embedded Linux distributions (Yocto / Buildroot /Debian)
- Custom operating systems and RTOS configurations for real-time requirements
- Driver integration, hardware bring-up and boot optimization

FPGA IP Development for signal / image processing

- Custom HDL IP for video acquisition and pre-processing
- Signal and image processing pipelines in programmable logic
- DSP blocks, filters, conversions and resize at deterministic latency
- AI accelerator integration into the FPGA data-path

FLEXIBLE PLATFORM · MULTI-SECTOR · EMBEDDED AI

ZU-NEXUS-AI in Summary

01 ZYNQ ULTRASCALE + AI NEXUS

The Zynq UltraScale+ multiprocessor SoC combined with a dedicated 25 TOPS neural accelerator.

02 MULTI-SECTOR

A single platform for medical, railway, industrial and drones: high-value AI vision.

03 OPTIMAL PIPELINE

Deterministic FPGA pre-processing, NPU inference, multi-sensor fusion on CPU.

04 KED ENGINEERING

Linux BSP and custom OS, FPGA IP development for tailored signal/image processing.