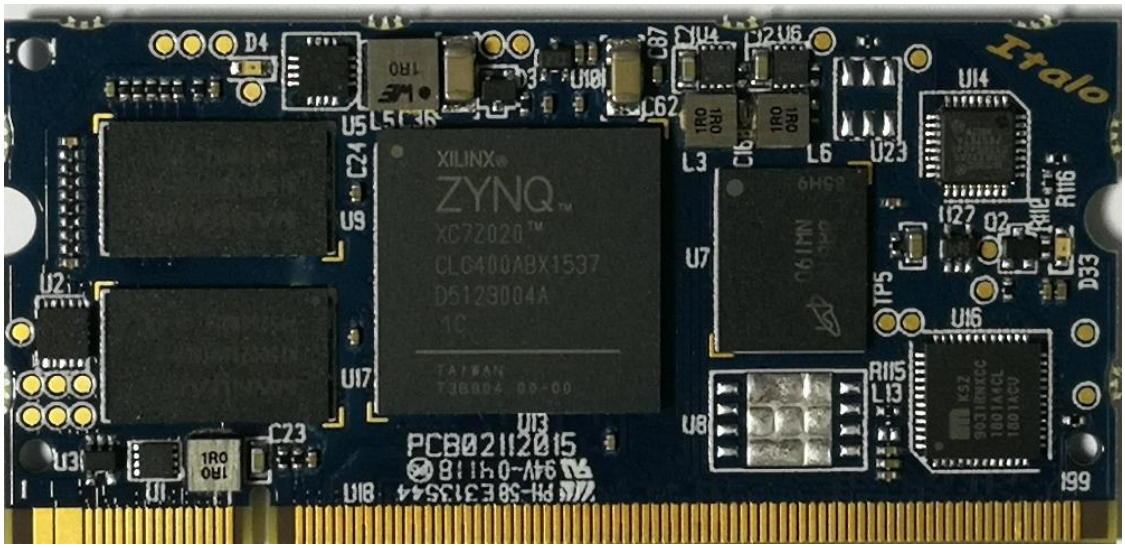
ELECTRONIC DESIGN

KED-ZYNQ-SOM

Hardware Reference Manual 1.0.1



INDEX OF REVISIONS		
Rev.	**Descriptions**	**Date (mm/dd/yyyy)**
V1_0_0	First Issue	11/25/2015
V1_0_1	Second Issue	12/02/2017

Table 1 – Index of Revisions

ELECTRONIC DESIGN

Contents

ELECTRONIC DESIGN

OVERVIEW

The KED-ZYNQ-SOM is an industrial-grade SoM (System on Module) based on Xilinx Zynq-7000 SoC (XC7Z020 or XC7Z014S or XC7Z010 or XC7Z007) with up to 1 GB of DDR3/L SDRAM, up to 32MB of SPI flash memory, 512MB of Nand Flash, Gigabit Ethernet PHY transceiver, a USB PHY transceiver and powerful switching-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via sodimm connector. See also Variants Currently in Production section.

KEY FEATURES

- Xilinx XC7Z SoC (XC7Z020, XC7Z014S, XC7Z010, XC7Z007)
- Processing system (PS):
- XC7Z020-XC7Z010: Dual-core ARM Cortex-A9 MPCore™ with CoreSight™
- XC7Z014S- XC7Z007S: Single-core ARM Cortex-A9 MPCore™ with CoreSight™
- L1 cache: 32 KByte instruction, 32 KByte data per processor
- L2 cache: Unified 512 KByte
- Programmable logic (PL): Artix-7 FPGA
- Programmable logic cells: 85K (XC7Z020), 65K (XC7Z014S) , 28K (XC7Z010) , 23K (XC7Z007S)
- Block RAM: 4.9 MByte (XC7Z020), 3.8 MByte (XC7Z014S) , 2.1 MByte (XC7Z010) , 1.8 MByte (XC7Z007S)
- DSP slices: 220 (XC7Z020), 170 (XC7Z014S) , 80 (XC7Z010) , 60 (XC7Z007S)
- Peak DSP performance: 276 GMACs (XC7Z020), 187 GMACs (XC7Z014S)
- 2x 12 bit, MSPS ADCs with up to 17 differential inputs
- 54 multiuse I/O (MIO) pins
- Up to 100 High-Range (HR) I/O pins (SelectIO interfaces)
- Up to 1 GByte DDR3/L SDRAM memory (2 x 256 Mbit x 16, 32-bit wide data bus).
- 32 MByte Quad SPI Flash memory
- 512Mbyte NAND Flash
- Gigabit Ethernet transceiver PHY (Microchip KSZ9031)
- MAC address serial EEPROM with EUI-48™ node identity (24AA02E48)
- Highly integrated full-featured hi-speed USB 2.0 ULPI transceiver (Microchip USB3320C-EZK)
- Power LED 1 (Green), FPGA DONE (Green)
- On-board high-efficiency DC-DC converters for all voltages used
- TYCO ELECTRONICS code 1473005-1 or compatible connector

Additional assembly options are available for cost or performance optimization upon request.

BLOCK DIAGRAM

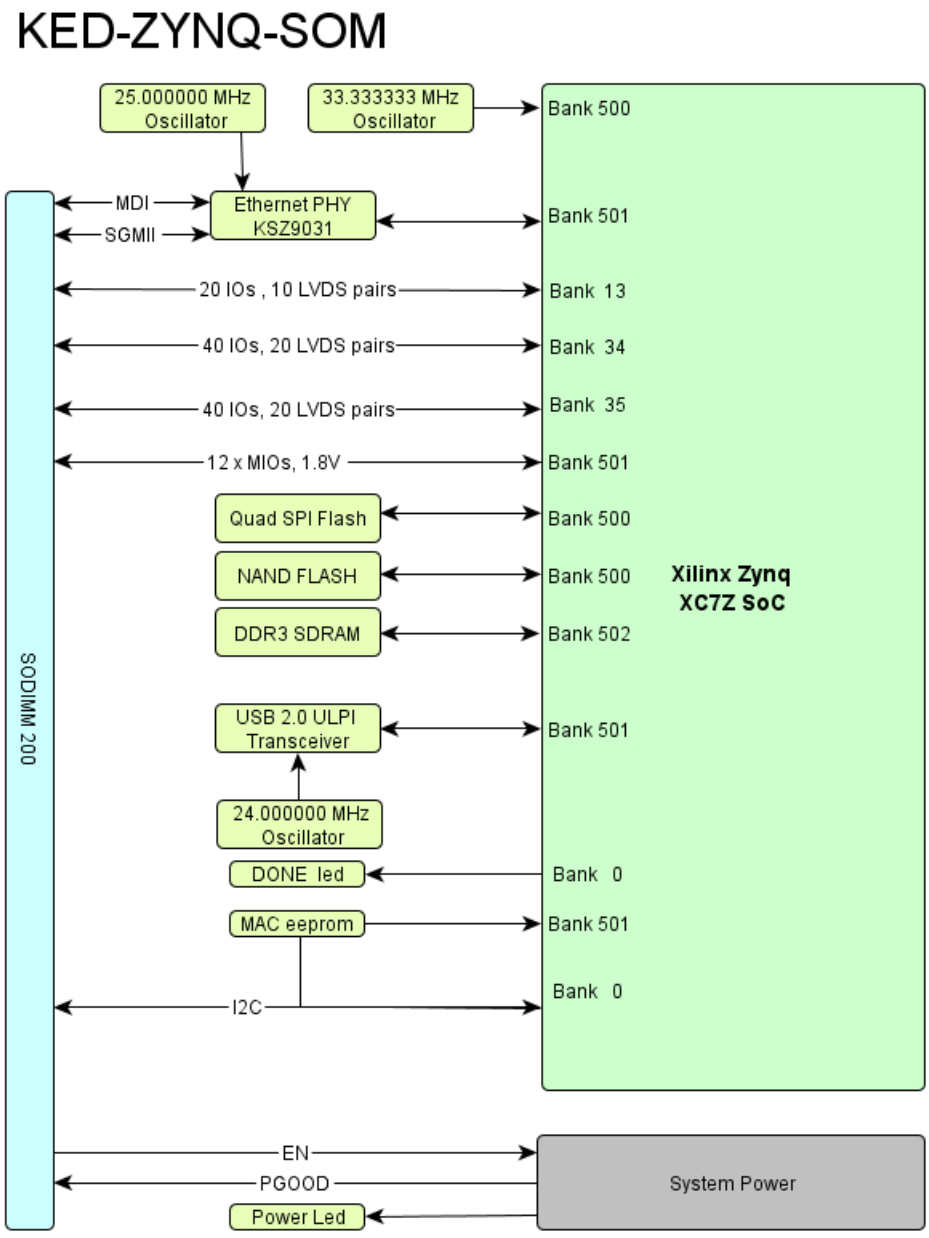
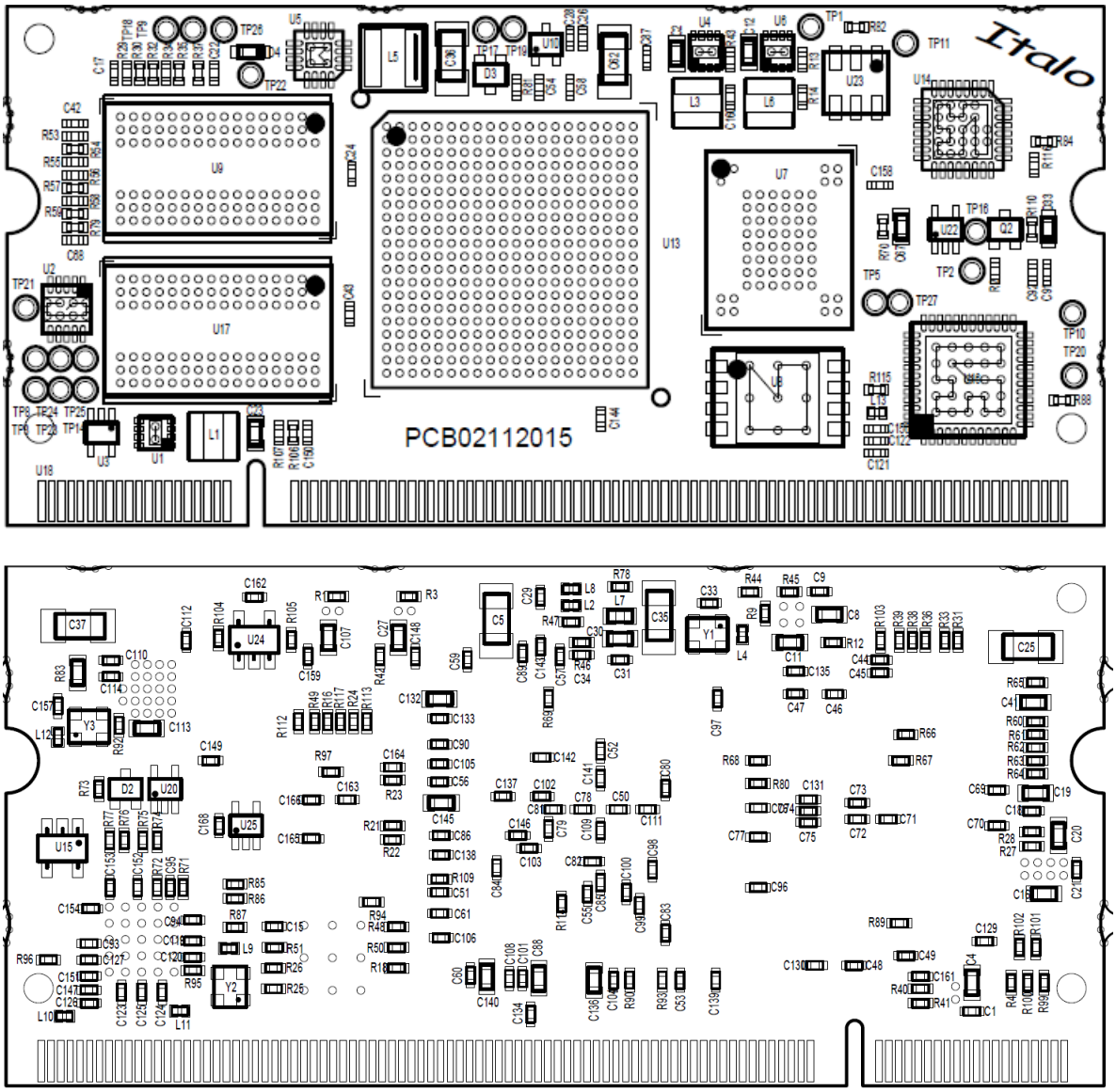


Figure 1: KED-ZYNQ-SOM block diagram.

MECHANICAL DATA

The KED-ZYNQ-SOM module has a standard SODIMM footprint compliant with TYCO ELECTRONICS code 1473005-1 or compatible connector.

The PCB dimensions is L 67.60 x W 32.1 x H 1 mm. The distances available on PCB under the module are from 1 to 1,5 mm 2.2 Assembly Top View The KED-ZYNQ-SOM Module has a Standard SODIMM footprint where odd pins are on top (component) side and even pins are on bottom side. The Figure below shows assembly and pin1 and pin 2 positions



MAIN COMPONENTS

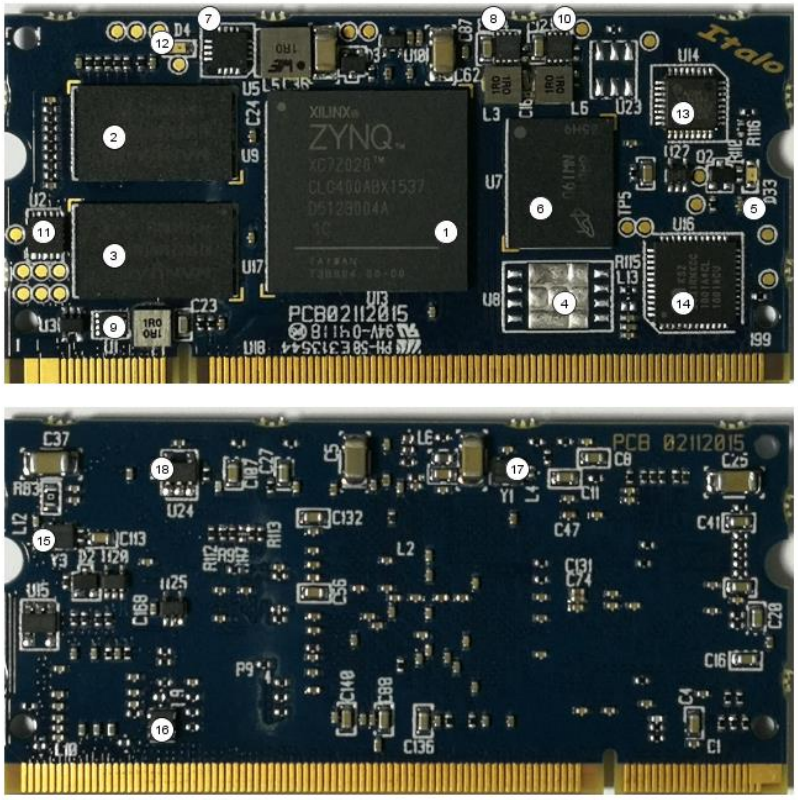


Figure 2: Main components of the module.

1. Xilinx Zynq XC7Z SoC, U13
2. 4 Gbit DDR3/L SDRAM, U9
3. 4 Gbit DDR3/L SDRAM, U17
4. 32 MByte Quad SPI Flash memory, U8
5. Green LED (PGOOD), D33
6. NAND Flash, U7
7. 4A high-efficiency PowerSoC DC-DC step-down converter (1V), U5
8. 2A high-efficiency PowerSoC DC-DC step-down converter (1.8V), U4
9. 2A high-efficiency PowerSoC DC-DC step-down converter (1.5V), U1
10. 2A high-efficiency PowerSoC DC-DC step-down converter (3.3V), U6
11. DDR termination regulator, U4
12. Green LED (DONE), D4
13. Hi-speed USB 2.0 ULPI transceiver, U14
14. Gigabit Ethernet (GbE) transceiver, U16
15. Low-power oscillator @ 24.000000 MHz (OTG-RCLK), Y3
16. Low-power oscillator @ 25.000000 MHz (ETH-CLK), Y2
17. Low-power oscillator @ 33.333333 MHz (PS-CLK), Y1
18. 2Kbit I2C serial EEPROM with EUI-48™ node identity, U24

PIN-OUT TABLES

PIN	CONNECTOR_NAME	FPGA_NAME	DESCRIPTION		PIN	CONNECTOR_NAME	FPGA_NAME	DESCRIPTION
1	GND	GND			2	GND	GND	
3	GND	GND			4	GND	GND	
5	5V0	5V0	SYSTEM POWER		6	5V0	5V0	SYSTEM POWER
7	5V0	5V0	SYSTEM POWER		8	5V0	5V0	SYSTEM POWER
9	5V0	5V0	SYSTEM POWER		10	3V3_SOM	3V3_SOM	
11	PWR_EN	PWR_EN	POWER ENABLE INPUT		12	TCK	TCK	JTAG
13	VCCIO_EN	VCCIO_EN	POWER GOOD OUT		14	TMS	TMS	JTAG
15	FPGA_SRST	FPGA_SRST	SOFTWARE RESET		16	TDI	TDI	JTAG
17	GND	GND			18	TDO	TDO	JTAG
19	GND	GND			20	GND	GND	
21	T5	IO_L19P_T3_13	FPGA_PIN		22	Y7	IO_L13P_T3_13	FPGA_PIN
23	U5	IO_L19N_T3_13	FPGA_PIN		24	Y6	IO_L13N_T3_13	FPGA_PIN
25	T9	IO_L12P_T3_13	FPGA_PIN		26	W11	IO_L18P_T3_13	FPGA_PIN
27	U10	IO_L12N_T3_13	FPGA_PIN		28	Y11	IO_L18N_T3_13	FPGA_PIN
29	GND				30	GND	GND	
31	V6	IO_L22P_T3_13	FPGA_PIN		32	V8	IO_L15P_T3_13	FPGA_PIN
33	W6	IO_L22N_T3_13	FPGA_PIN		34	W8	IO_L15N_T3_13	FPGA_PIN
35	Y9	IO_L14P_T3_13	FPGA_PIN		36	W10	IO_L16P_T3_13	FPGA_PIN
37	Y8	IO_L14N_T3_13	FPGA_PIN		38	W9	IO_L16N_T3_13	FPGA_PIN
39	1V5_SOM	1V5_SOM			40	GND	GND	
41	VCCIO_B13	VCCIO_B13			42	VCCIO_B13	VCCIO_B13	
43	V11	IO_L21P_T3_13	FPGA_PIN		44	Y12	IO_L20P_T3_13	FPGA_PIN
45	V10	IO_L21N_T3_13	FPGA_PIN		46	Y13	IO_L20N_T3_13	FPGA_PIN
47	GND	GND			48	GND	GND	
49	U13	IO_L3P_T0_DQS_PUDC_B_34	FPGA_PIN		50	V12	IO_L4P_T0_34	FPGA_PIN
51	V13	IO_L3N_T0_DQS_34	FPGA_PIN		52	W13	IO_L4N_T0_34	FPGA_PIN
53	W14	IO_L8P_T1_34	FPGA_PIN		54	U14	IO_L11P_T1_SRCC_34	FPGA_PIN
55	Y14	IO_L8N_T1_34	FPGA_PIN		56	U15	IO_L11N_T1_SRCC_34	FPGA_PIN
57	GND	GND			58	GND	GND	
59	T14	IO_L5P_T0_34	FPGA_PIN		60	V16	IO_L18P_T2_34	FPGA_PIN
61	T15	IO_L5N_T0_34	FPGA_PIN		62	W16	IO_L18N_T2_34	FPGA_PIN
63	Y16	IO_L7P_T1_34	FPGA_PIN		64	T16	IO_L9P_T1_DQS_34	FPGA_PIN
65	Y17	IO_L7N_T1_34	FPGA_PIN		66	U17	IO_L9N_T1_DQS_34	FPGA_PIN
67	GND	GND			68	GND	GND	
69	V17	IO_L21P_T3_DQS_34	FPGA_PIN		70	U18	IO_L12P_T1_MRCC_34	FPGA_PIN
71	V18	IO_L21N_T3_DQS_34	FPGA_PIN		72	U19	IO_L12N_T1_MRCC_34	FPGA_PIN
73	Y18	IO_L17P_T2_34	FPGA_PIN		74	V20	IO_L16P_T2_34	FPGA_PIN
75	Y19	IO_L17N_T2_34	FPGA_PIN		76	W20	IO_L16N_T2_34	FPGA_PIN
77	VCCIO_B34	VCCIO_B34			78	VCCIO_B34	VCCIO_B34	

79	P14	IO_L6P_T0_34	FPGA_PIN	80	T20	IO_L15P_T2_DQS_34	FPGA_PIN
81	R14	IO_L6P_T0_VREF_34	FPGA_PIN	82	U20	IO_L15N_T2_DQS_34	FPGA_PIN
83	V15	IO_L10P_T1_34	FPGA_PIN	84	R16	IO_L19P_T3_34	FPGA_PIN
85	W15	IO_L10N_T1_34	FPGA_PIN	86	R17	IO_L19N_T3_34	FPGA_PIN
87	VCCIO_B34	VCCIO_B34		88	VCCIO_B34	VCCIO_B34	
89	W18	IO_L22P_T3_34	FPGA_PIN	90	N20	IO_L14P_T2_SRCC_34	FPGA_PIN
91	W19	IO_L22N_T3_34	FPGA_PIN	92	P20	IO_L14N_T2_SRCC_34	FPGA_PIN
93	N18	IO_L13P_T2_MRCC_34	FPGA_PIN	94	T17	IO_L20P_T3_34	FPGA_PIN
95	P19	IO_L13N_T2_MRCC_34	FPGA_PIN	96	R18	IO_L20N_T3_34	FPGA_PIN
97	GND	GND		98	GND	GND	
99	1V0_SOM	1V0_SOM		100	1V0_SOM	1V0_SOM	
101	K16	IO_L24P_T3_AD15P_35	FPGA_PIN	102	M17	IO_L8P_T1_AD10P_35	FPGA_PIN
103	J16	IO_L24N_T3_AD15N_35	FPGA_PIN	104	M18	IO_L8N_T1_AD10N_35	FPGA_PIN
105	L19	IO_L9P_T1_DQS_AD3P_35	FPGA_PIN	106	M19	IO_L7P_T1_AD2P_35	FPGA_PIN
107	L20	IO_L9N_T1_DQS_AD3N_35	FPGA_PIN	108	M20	IO_L7N_T1_AD2N_35	FPGA_PIN
109	GND	GND		110	GND	GND	
111	J20	IO_L17P_T2_AD5P_35	FPGA_PIN	112	K17	IO_L12P_T1_MRCC_35	FPGA_PIN
113	H20	IO_L17N_T2_AD5N_35	FPGA_PIN	114	K18	IO_L12N_T1_MRCC_35	FPGA_PIN
115	F19	IO_L15P_T2_DQS_AD12P_35	FPGA_PIN	116	L16	IO_L11P_T1_SRCC_35	FPGA_PIN
117	F20	IO_L15N_T2_DQS_AD12N_35	FPGA_PIN	118	L17	IO_L11N_T1_SRCC_35	FPGA_PIN
119	GND	GND		120	GND	GND	
121	D19	IO_L4P_T0_35	FPGA_PIN	122	H16	IO_L13P_T2_MRCC_35	FPGA_PIN
123	D20	IO_L4N_T0_35	FPGA_PIN	124	H17	IO_L13N_T2_MRCC_35	FPGA_PIN
125	C20	IO_L1P_T0_AD0P_35	FPGA_PIN	126	J18	IO_L14P_T2_AD4P_SRCC_35	FPGA_PIN
127	B20	IO_L1N_T0_AD0N_35	FPGA_PIN	128	H18	IO_L14N_T2_AD4N_SRCC_35	FPGA_PIN
129	VCCIO_B35	VCCIO_B35		130	VCCIO_B35	VCCIO_B35	
131	K19	IO_L10P_T1_AD11P_35	FPGA_PIN	132	F16	IO_L6P_T0_35	FPGA_PIN
133	J19	IO_L10N_T1_AD11N_35	FPGA_PIN	134	F17	IO_L6N_T0_35	FPGA_PIN
135	G19	IO_L18P_T2_AD13P_35	FPGA_PIN	136	E18	IO_L5P_T0_AD9P_35	FPGA_PIN
137	G20	IO_L18N_T2_AD13N_35	FPGA_PIN	138	E19	IO_L5N_T0_AD9N_35	FPGA_PIN
139	VCCIO_B35	VCCIO_B35		140	VCCIO_B35	VCCIO_B35	
141	H15	IO_L19P_T3_35	FPGA_PIN	142	B19	IO_L2P_T0_AD8P_35	FPGA_PIN
143	G15	IO_L19N_T3_VREF_35	FPGA_PIN	144	A20	IO_L2N_T0_AD8N_35	FPGA_PIN
145	G17	IO_L16P_T2_35	FPGA_PIN	146	E17	IO_L3P_T0_DQS_AD1P_35	FPGA_PIN
147	G18	IO_L16N_T2_35	FPGA_PIN	148	D18	IO_L3N_T0_DQS_AD1N_35	FPGA_PIN
149	GND	GND		150	GND	GND	
151	FPGA_VP	FPGA_VP		152	SD_CLK	PS_MIO40	
153	FPGA_VN	FPGA_VN		154	SD_CMD	PS_MIO41	
155	UART0_RX	PS_MIO50		156	SD_DATA0	PS_MIO42	
157	UART0_TX	PS_MIO51		158	SD_DATA1	PS_MIO43	
159	I2C1_SCL	PS_MIO48		160	SD_DATA2	PS_MIO44	
161	I2C1_SDA	PS_MIO49		162	SD_DATA3	PS_MIO45	
163	ONE_WIRE	ONE_WIRE		164	SD_WPn	PS_MIO47	
165	GND	GND		166	SD_CDn	PS_MIO46	

167	ETH_CTRL_REF	ETH_CTRL_REF			168	1V8_SOM	1V8_SOM	
169	ETH_A_P	ETH_A_P			170	FPGA_PORn	FPGA_PORn	
171	ETH_A_N	ETH_A_N			172	GND	GND	
173	GND	GND			174	FLASH_CSn	PS_MIO_1	
175	ETH_B_P	ETH_B_P			176	FLASH_SDO	PS_MIO_3	
177	ETH_B_N	ETH_B_N			178	FLASH_SDI	PS_MIO_2	
179	GND	GND			180	FLASH_SCLK	PS_MIO_6	
181	ETH_C_P	ETH_C_P			182	BOOT_MODE0	PS_MIO_4	BOOT_MODE
183	ETH_C_N	ETH_C_N			184	BOOT_MODE1	PS_MIO_5	BOOT_MODE
185	GND	GND			186	1V8_SOM	1V8_SOM	
187	ETH_D_P	ETH_D_P			188	OTG_CPEN	OTG_CPEN	
189	ETH_D_N	ETH_D_N			190	OTG_D_P	OTG_D_P	
191	GND	GND			192	OTG_D_N	OTG_D_N	
193	ETH_LED2	ETH_LED2			194	OTG_VBUS	OTG_VBUS	
195	ETH_LED1	ETH_LED1			196	OTG_ID	OTG_ID	
197	3V3_SOM	3V3_SOM			198	GND	GND	
199	3V3_SOM	3V3_SOM			200	VBATT	VBATT	

INITIAL DELIVERY STATE

Storage device name	IC	Content	Notes
Quad SPI Flash	U8	Empty	-
NAND Flash	U7	Empty	-
24AA02E48T EEPROM	U24	Pre-programmed globally unique, 48-bit node address (MAC)	-

Table 1: Initial state of programmable devices on delivery of the module.

BOOT PROCESS

By default the KED-ZYNQ-SOM supports QSPI, NAND Flash, and SD Card boot modes which is controlled by the BOOT0 and BOOT1 input signal from the SODIMM connector.

BOOT_MODE1	BOOT_MODE0	Boot Mode
Low	Low	JTAG
Low	High	NAND
High	Low	QSPI
Low	Low	SDCARD

Table 14: Boot modes.

SIGNALS, INTERFACES AND PINS

SODIMM I/OS

PL I/O signal connections between Zynq SoC's I/O banks and SoDimm connectors, up to 100HR GPIOs total.

Bank	Type	Voltage	I/O Count	Notes
13	HR GPIO	VCCIO13	20	10 LVDS pairs
34	HR GPIO	VCCIO34	40	20 LVDS pairs
35	HR GPIO	VCCIO35	40	20 LVDS pairs

Table 2: General PL I/O to SoDimm connectors information.

PS MIO bank 501 signal connections to SoDimm connector, 12 PS MIOs total.

MIO	SoDimm Pin	Bank	Voltage	Notes
MIO40	152	501	1.8V	Zynq SoC SDCARD
MIO41	154	501	1.8V	Zynq SoC SDCARD
MIO42	156	501	1.8V	Zynq SoC SDCARD
MIO43	158	501	1.8V	Zynq SoC SDCARD
MIO44	160	501	1.8V	Zynq SoC SDCARD
MIO45	162	501	1.8V	Zynq SoC SDCARD
MIO46	166	501	1.8V	Zynq SoC SD0
MIO47	164	501	1.8V	Zynq SoC SD0
MIO48	159	501	1.8V	Zynq SoC I2C1
MIO49	161	501	3.3V	Zynq SoC I2C1
MIO50	155	501	1.8V	Zynq SoC UART0
MIO51	157	501	1.8V	Zynq SoC UART0

Table 3: General PS MIO connections information.

JTAG INTERFACE

JTAG access to the Zynq SoC is provided through SoDimm connector

JTAG Signal	SoDimm Connector Pin
TMS	14
TDI	16
TDO	18
TCK	12

Table 4: JTAG pins connection.

QUAD SPI INTERFACE

Quad SPI Flash (U8) is connected to the Zynq PS QSPI0 interface via PS MIO bank 500, pins MIO1..6.

MIO	Signal Name
1	SPI-CS
2	SPI-DQ0/M0
3	SPI-DQ1/M1
4	SPI-DQ2/M2
5	SPI-DQ3/M3
6	SPI-SCK/M4

Table 6: Quad SPI interface MIOs and pins.

NAND FLASH INTERFACE

The KED-ZYNQ-SOM has on-board Nand Flash memory device (U7), some pin are shared with QSPI

MIO	Signal Name
0	NAND_CSn
2	NAND_ALE
3	NAND_WE
4	NAND_DATA2
5	NAND_DATA0
6	NAND_DATA1
7	NAND_CLE
8	NAND_RE
9	NAND_DATA4
10	NAND_DATA5
11	NAND_DATA6
12	NAND_DATA7
13	NAND_DATA3
13	NAND_BUSY

Table 7: NAND interface MIOs and pins.

ETHERNET INTERFACE

The Micrel KSZ9031 (U16) is a physical layer device containing a single Gigabit Ethernet transceiver and three separate major electrical interfaces: MDI interface to copper cable, SGMII interface and RGMII interface. RGMII interface is connected to the Zynq SoC PS bank 501 MIO pins, see tables below.

SGMII (SFP copper) pins and MDI pins are routed to the SoDimm connector

ETHERNET PHY TO SODIMM CONNECTIONS

PHY Signal	SoDimm Pin
PHY_MDI0_P	169
PHY_MDI0_N	171
PHY_MDI1_P	175
PHY_MDI1_N	177
PHY_MDI2_P	181
PHY_MDI2_N	183
PHY_MDI3_P	187
PHY_MDI3_N	189

Table 8: Ethernet PHY to SoDimm connections.

ETHERNET PHY TO ZYNQ SOC PS MIO ETH0 CONNECTIONS

PHY Signal	SoC MIO		PHY Signal	SoC MIO
ETH-TXCK	16		ETH-RXCK	22
ETH-TXD0	17		ETH-RXD0	23

PHY Signal	SoC MIO		PHY Signal	SoC MIO
ETH-TXD1	18		ETH-RXD1	24
ETH-TXD2	19		ETH-RXD2	25
ETH-TXD3	20		ETH-RXD3	26
ETH-TXCTL	21		ETH-RXCTL	27
ETH-MDC	52		ETH-MDIO	53

Table 9: Ethernet PHY to Zynq SoC connections.

USB INTERFACE

Hi-speed USB ULPI PHY is provided by USB3320 from Microchip (U18). The ULPI interface is connected to the Zynq SoC PS USB0 via MIO28..39, bank 501.

USB PHY Signal	Wired to	SoC MIO
OTG-DATA4	U14-7	28
OTG-DIR	U14-31	29
OTG-STP	U14-29	30
OTG-NXT	U14-2	31
OTG-DATA0	U14-3	32
OTG-DATA1	U14-4	33
OTG-DATA2	U14-5	34

USB PHY Signal	Wired to	SoC MIO
OTG-DATA3	U14-6	35
OTG-CLK	U14-1	36
OTG-DATA5	U14-9	37
OTG-DATA6	U14-10	38
OTG-DATA7	U14-13	39

Table 10: USB ULPI PHY to Zynq SoC connections.

USB PHY connection

USB PHY Pin	MIO	SoDimm Name	Notes
RESETB	MIO15	-	Active low reset.
CLKOUT	MIO15	-	ULPI output clock connected to Zynq PS MIO36.
DP, DM		OTG_D_P,OTG_D_N	USB data lines.
CPEN		OTG_CPEN	External USB power switch active high enable signal.
VBUS	-	OTG_VBUS	Connect to USB VBUS via a series of resistors
ID	-	OTG_ID	For A-device connect to the ground, for B-device leave floating.

Table 11: USB ULPI PHY connections.

I2C INTERFACE

On-board I2C devices are connected to the Zynq SoC.

Signal Name	SoC Pin	Notes
I2C1_SCL1	MIO48	SCL, I2C clock.
I2C1_SDA1	MIO49	SDA, I2C data out.

Table 12: Zynq SoC I^2C bus.

I^2C Device	I^2C Address	IC	Notes
24AA02E48	0x50	U24	EEPROM

Table 13: I2C slave device addresses.

ON-BOARD PERIPHERALS

DDR MEMORY

By default KED-ZYNQ-SOM module has two DDR3/L SDRAM chips arranged into 32-bit wide memory bus providing total on-board memory size up to 1 GBytes. Size of memory depends on the module variant, refer to the variants table.

QUAD SPI FLASH MEMORY

On-board 32-MByte QSPI flash memory S25FL256S (U8) is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

NAND FLASH MEMORY

NAND Flash memory device(U15) is connected to the Zynq PS MIO bank 501 pins (see also Variants Currently in Production for options). Depending on the module variant, different make and model of NAND chips are available.

GIGABIT ETHERNET PHY

On-board Gigabit Ethernet PHY is provided with Microchip KSZ9031 IC (U16). The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signalling. The reference clock input of the PHY is supplied from an on-board 25.000000 MHz oscillator (Y2).

PHY Signal	SoDimm Pin
PHY_LED0	193
PHY_LED1	193

Table 15: Ethernet LED connections.

HIGH-SPEED USB ULPI PHY

Hi-speed USB ULPI PHY is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0 via MIO28..39, bank 501 (see also section. The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 24.000000 MHz oscillator (Y3).

MAC-ADDRESS EEPROM

A Microchip 2Kbit 24AA02E48 serial EEPROM (U24) is connected to the Zynq PS pin via I2C serial interface and contains pre-programmed globally unique 48-bit node address compatible with EUI-48TM specification. Chip is programmed at the factory with a globally unique node address stored in the upper 1/4 of the memory array and write-protected through the STATUS register. The remaining 1,536 bits are available for application use.

OSCILLATORS

Source	Signal	Frequency	Destination	Pin Name	Notes
Y1	PS-CLK	33.333333 MHz	U13	PS_CLK_500	Zynq SoC PS subsystem main clock.
Y3	OTG-RCLK	24.000000 MHz	U14	REFCLK	USB3320C PHY reference clock.
Y2	ETH-CLK	25.000000 MHz	U16	XTAL_IN	88E1512 PHY reference clock.

Table 16: Oscillators.

ON-BOARD LEDS

LED	Color	Connected to	Description and Notes
D4	Green	DONE	
D33	GREEN	Power Good	Controlled by reset controller TPS3801E18 .

Table 17: On-board LEDs.

POWER AND POWER-ON SEQUENCE

Power Supply

Power supply with minimum current capability of 3A for system startup is recommended.

Power Consumption

Power Input Pin	Typical Current
VIN	TBD*

Table 18: Power Consumption.

* TBD - To Be Determined.

Power Distribution Diagram

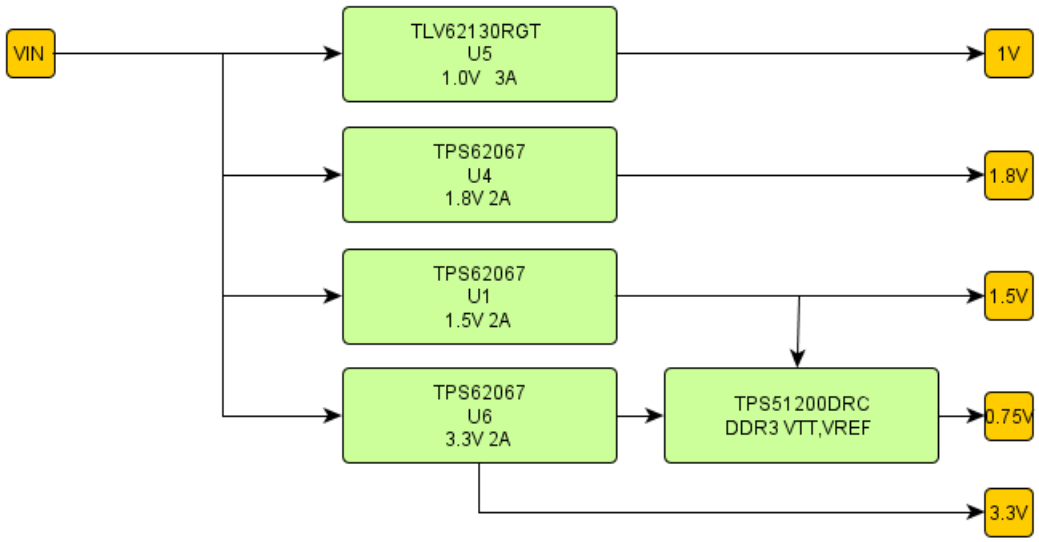


Figure 3: Power distribution diagram.

Power-On Sequence

It is important that all carrier board I/Os are 3-stated at power-on until the module sets the power good signal high (VCCIO_EN on the SoDimm Connector) meaning that all on-module voltages have become stable and module is properly powered up.

Use 3.3V or 1.8V output to enable external power supplies or power switches which are used to supply FPGA banks.

See also Xilinx datasheet DS187 for additional information. User should also check related carrier board documentation when choosing carrier board design for KED-ZYNQ-SOM module.

PWR_EN input signal

PWR_EN input signal from the carrier board must be used to enable power up of the module. This pin is internally pullup, so if unuset left floating.

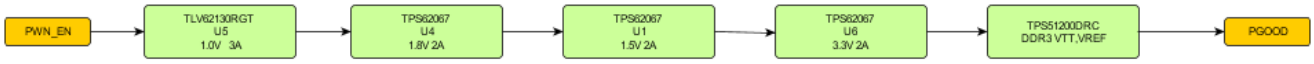


Figure 4: Power sequencing.

Power Rails

SoDimm Name	SoDimm Pins	Direction	Note
VIN	5,7,9,6,8	Input	Supply voltage from carrier board.
JTAG VREF	10	Output	JTAG reference voltage. Attention: Net name on schematic is "3.3VIN"
VCCIO35	129,139,130,140	Input	High range bank voltage from carrier board.
VCCIO13	41,42	Input	High range bank voltage from carrier board.
VCCIO34	77,87,78,88	Input	High range bank voltage from carrier board.
VBAT_IN	200	Input	FPGA VBAT supply voltage.
3.3V	197,199	Output	Internal 3.3V voltage level.
1.8V	168,186	Output	Internal 1.8V voltage level.
1.5V	39	Output	Internal 1.5V voltage level.
1.0V	99,100	Output	Internal 1.0V voltage level.

Table 19: Module power rails.

Bank Voltages

Bank	Schematic Name	Voltage	Notes
500	1.8V, VCCO_MIO0_500	1.8V	
501	1.8V, VCCO_MIO1_501	1.8V	

Bank	Schematic Name	Voltage	Notes
502	1.5V, VCCO_DDR_502	1.5V	
0 Config	3.3V	3.3V	
13 HR	VCCO13	1.2V to 3.3V	Supplied by the carrier board.
34 HR	VCCIO34	1.25V to 3.3V	Supplied by the carrier board.
35 HR	VCCIO35	1.2V to 3.3V	Supplied by the carrier board.

Table 20: Zynq SoC bank voltages.

Variants Currently in Production

Module Variant	Zynq SoC	RAM	NAND Size	Temperature Range
KED-Z20-1G-512M-C	XC7Z020-1CLG400C	1 GByte	4 GBit	Commercial
KED-Z20-1G-512M-I	XC7Z020-1CLG400I	1 GByte	4 GBit	Industrial
KED-Z14-1G-512M-C	XC7Z014S-1CLG400C	1 GByte	4 GBit	Commercial
KED-Z14-1G-512M-I	XC7Z014S-1CLG400I	1 GByte	4 GBit	Industrial
KED-Z10-512M-512M-C	XC7Z010-1CLG400C	512 MByte	4 GBit	Commercial
KED-Z10-512M-512M-C	XC7Z010-1CLG400I	512 MByte	4 GBit	Industrial
KED-Z07-512M-512M-C	XC7Z007S-1CLG400C	512 MByte	4 GBit	Commercial

Module Variant	Zynq SoC	RAM	NAND Size	Temperature Range
KED-Z07-512M-512M-C	XC7Z007S-1CLG400I	512 MByte	4 GBit	Industrial

Table 21: Module variants currently in production.

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	-0.3	6	V	TLV62130RGT datasheet.
Supply voltage for PS MIO banks	-0.5	1.8	V	See Xilinx DS187 datasheet.
I/O input voltage for MIO banks	-0.4	VCCO_MIO + 0.55	V	See Xilinx DS187 datasheet. (VCCO_MIO0_500, VCCO_MIO1_501)
Supply voltage for HR I/Os banks	-0.5	3.6	V	See Xilinx DS187 datasheet. (VCCIO13, VCCIO34, VCCIO35)
I/O input voltage for HR I/O banks	-0.4	VCCIO + 0.55	V	See Xilinx DS187 datasheet.
Storage temperature	-40	+85	°C	-

Table 22: Module absolute maximum ratings.

Assembly variants for higher storage temperature range are available on request.

Please check Xilinx datasheet DS187 for complete list of absolute maximum and recommended operating ratings.

Recommended Operating Conditions

Table 23: Recommended operating conditions.

Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial and automotive grade: -40°C to +85°C.

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Revision History

Hardware Revision History

Date	Revision	Notes	PCN
2015-10-12	03		
-	02		
-	01	Prototypes	

Table 24: Hardware revision history table.

There is no hardware revision number marking on the module PCB.

Document Change History

Date	Revision	Contributors	Description
2015-08-31	v.83	Rodolfo Facchini	Initial document.
--	all	Rodolfo Facchini, Erika Magrini	--

Table 25: Document change history table.

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